CPT-Mini2810 Card

Technical Manual

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Revision History of the CPT-Mini2810 Interface Board

Card Revision 1.0:

Version 1.0 - Initial Release

Card Revision 1.1:

Version 1.1 - Major restructuring of the board to remove the test functionality.
Added CPLD
Added Hysteresis Controller functionality
– basic manual only to mention capability
Added Multiplexer for analog inputs
Added DACs (4 x external, 4 x internal)
Removed Isolated RS-232/485 interfaces
Technical Brief released only

Version 1.2 - Full Release of Technical Manual

Version 1.3 - Added PWM output enable to CPLD EVACOMCON register bit 0 (ENA)
Added PWM output enable to CPLD EVBCOMCON register bit 0 (ENB)
Restructured CPLD code – V2.0

Version 1.4 - Restructured CPLD code – V2.1 and above
Added DATEHI, DATELO, VERSION and SPECIAL registers

Version 1.5: Corrected error in Table 3-19 relating to DIGIN1-4 definitions
Corrected corresponding error in Appendix D pinout definitions
Acknowledgement to Zaki for finding the error.

Version 1.6: Corrected definition of default conditions for CPLD GPIO Register
Corrected definition error of ANLGSW register in Appendix
Added caution about the operation of the SPD bit in the SCIBMODE register.
Added default values for CPLD registers at reset to Register Appendices

Table of Contents

CPT-Mini2810 Board

1.0 Overview of the CPT-Mini2810 Board

The CPT-Mini2810 interface board is part of the third-generation processor boards based on the MINI MICRO card series. Used in conjunction with the CPT-DA2810 DSP processor card, it provides a low cost, high performance DSP based controller, intended specifically for applications where a discrete BUS based system would be too expensive, and where time/money/resource constraints make a custom design impracticable. The card is designed around a plug-in CPT-DA2810 circuit board that utilises Texas Instruments TMS320F2810 or TMS320F2811 DSP chips, which have been specifically optimised for use in digital motor/motion control applications. This DSP is capable of running with a 150MHz system clock.

The CPT-Mini2810 interface card measures 202mm x 73mm and has 8 major sections:

- CPT-DA2810 plug-in,
- MINI BUS interface,
- Analog Inputs,
- PWM Outputs,
- Digital I/O,
- DAC Outputs
- Altera MAX II CPLD
- Optional Hysteresis Controller
- Communications
- Ancillary support circuitry.

The board is designed to plug into a custom-designed motherboard (such as a CS-IIB, CS-GIIB or CS-IIC also available from Creative Power Technologies).

The plug-in card requires regulated +/-15V and 5V supplies to be provided from off-card.

On-card facilities include:

- A CPT-DA2810socket
- 1 x TTL level serial interface with transmit control functionality (off-card RS-422/485 capable)
- 1 x TTL level serial interface
- 4 wire clocked serial port (can be configured for master/slave operation)
- 1 off 16-bit TTL digital I/O ribbon connector, supporting 2 off 8 bit I/O banks
- 16 off single ended analog inputs
- Configurable hysteresis band controller
- 8 bit MINI bus interface (INTEL iSBX compatible)
- 6 bit TTL digital input / external interrupt port
- JTAG Programmable MAX II EPM570T100C5N CPLD
- 8 PWM outputs, arranged as 3 off complementary pairs and 2 off independent outputs
- 8 selectable PWM outputs, arranged as 3 off complementary pairs and 2 off independent outputs
- 4 DAC outputs (±10V)
- On-card voltage regulation

Figure 1-1 is a functional block diagram of the CPT-Mini2810 controller card, showing all major sections.

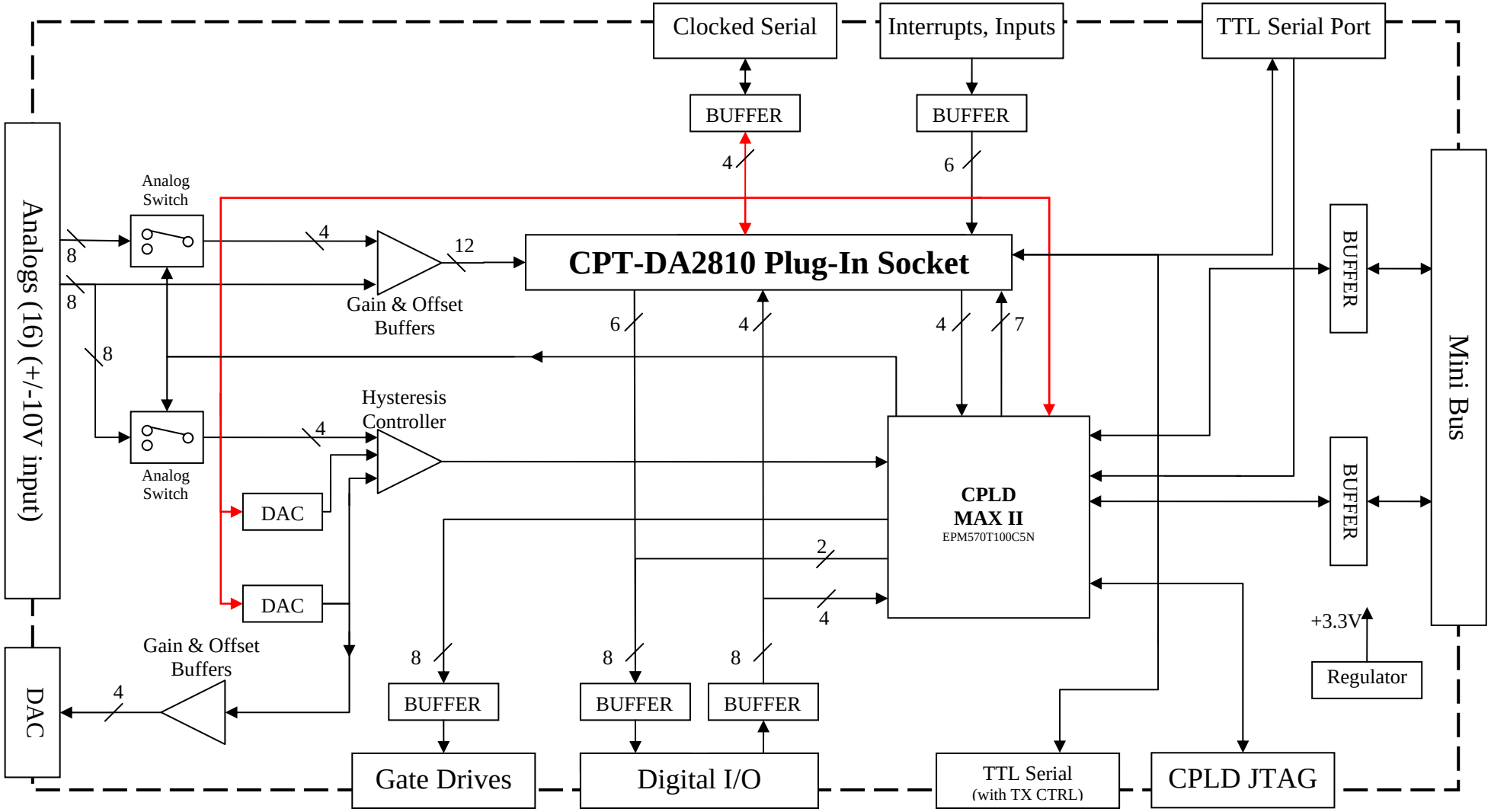


Figure 1-1: Functional Diagram of CPT-Mini2810 Board

1.1 CPT-DA2810 Interface

The CPT-Mini2810 requires a plug-in controller card to operate. There is an 80 way IDC header located in the centre of the board for connection to a CPT-DA2810, or equivalent, processor board. All signals on the CPT-Mini2810 are correctly buffered to interface with the CPT-DA2810 board.

1.2 Digital I/O

The CPT-Mini2810 supports 16 bits of digital I/O, arranged as 1 port of 8 bits digital output and 1 port of 8 bits digital input. DSP I/O pins B0-B7 form one TTL level digital output bank and the digital input bank is shared among I/O pins on DSP ports A, B and the CPLD. Access is via a buffered 20-way IDC header connector (ribbon cable type connector). Digital Ground and +5V connections are also brought out to this connector for use by external interface circuitry. Four of the digital inputs can be selected within the CPLD to interface to different capture ports on the DSP.

The eight digital outputs can also be configured as PWM outputs on Event Manager B (EVB).

Six TTL level buffered external interrupts are also provided through a separate 16-way IDC header.

1.3 Analog Inputs

The 16 off analog inputs accept a ±10V input through a 26-way IDC header connector (normal ribbon cable type connector). Due to the need for explicit external calibration of the TMS320F2810 ADC module only 12 analog inputs can be accessed at any given time. The 26-way header has been retained to provide full compatibility with the existing CS-MiniDSP peripheral range. Selection of the active analog channels is achieved on-card by changeover analog switches. Eight of the analog inputs are selectable through analog switches to feed into four DSP analog channels.

The TMS320F2810 has a 12-bit A/D converter with two built-in Sample and Hold circuits. This enables two input channels, one on each ADC unit, to be sampled and converted almost “simultaneously” in a pipelined process. The DSP A/D converter accepts input voltages in the range of 0-3V. Conditioning circuits are provided on the CPT-Mini2810 to translate the incoming ±10V to 0-3V. Glitch filtering and diode clamps are located on the CPT-DA2810 as they are best placed next to the DSP pins to minimise noise injection and to protect the DSP inputs.

In addition, two banks of 4 analog inputs (4 voltage or 4 current) can be fed to the hysteresis controller circuitry (not loaded by default) located on-card. Analog switches are used to select the source for each signal.

1.4 Gate Drive Interface

The CPT-Mini2810 interface board supports 16 PWM outputs, 8 off available on a 16-way gate drive interface sourced from Event Manager A (EVA), and 8 off shared with the digital I/O connector sourced from Event Manger B (EVB).

The EVA 16-way gate drive connector has buffered TTL level PWM outputs for connection to an external gate driver board. The port supports 8 PWM outputs, which can be sourced from either the 80-way CPT-DA2810 interface or via the on-card hysteresis controller.

Event Manager A PWM outputs are made up of 3 complementary pairs (6 outputs) with programmable deadbands and 2 independent outputs generated by simple compare units. The simple compare units can be paired within the CPLD to create complementary signals and to introduce a programmable deadband.

The hysteresis controller generates PWM gate signals from the on-card circuitry via the CPLD outputs. The default version of the CPT-Mini2810 does not have the hysteresis controller functionality loaded.

Fault monitoring for EVA is supported using the PDPINTA* external interrupt, which causes the PWM outputs to enter a low state in the event of a fault. This is a hardware-triggered function within the DSP and is available on the 16-way interrupts connector.

Event Manager B (EVB), which is available via the CPT-DA2810 80 way interface, can also be configured in PWM mode. It is available for off-card use through the digital I/O interface connector. Fault monitoring for EVB is supported using the PDPINTB* external interrupt, which is available on the interrupts 16-way connector.

1.5 Analog Outputs

There are 4 off external analog outputs on the CPT-Mini2810 that are produced from a quad 12-bit *nano*DAC®. Each DAC output is conditioned to produce a bipolar output (±10V). All DAC outputs are fed to a single 10-way IDC header. The DACs are accessed via the SPI.

Four off additional analog outputs can be loaded and used, in conjunction with the external DACs, when the hysteresis controller functionality is active. This DAC and associated circuitry are not loaded on the default CPT-Mini2810 board.

1.6 Communications

The CPT-Mini2810 interface board has one off asynchronous serial port and a 4-wire serial peripheral interface (SPI). The asynchronous serial port can be configured to operate through the CS-MiniDSP plug-in TTL compatible interface or, alternatively, to a dedicated connector capable of supporting an off-card RS-232/422/485 interface.

The SPI is available on the CS-MiniDSP plug-in footprint. The SPI is also used in master mode for on-card peripheral communication.

None of the communications ports are isolated on-card.

1.7 Hysteresis Controller

The CPT-Mini2810 has the provision for a four channel variable bandwidth closed loop hysteresis controller. Each hysteresis channel has a summing amplifier that creates an error signal from the difference between a target reference command and a feedback input. Each error signal feeds into a variable band hysteresis comparator that switches its output up and down as the error crosses lower and upper hysteresis boundaries. The comparator outputs feed into a CPLD, which allows additional logic such as crossover delays and lock out functions to be integrated with the comparator outputs before sending them on as gate command signals to the EVA PWM outputs to control a power electronic switching stage.

The target reference commands and hysteresis bandwidths are generated on card using eight 12 bit DACs, controlled by the CPT-DA2810 DSP controller. All four hysteresis channels are independent and essentially identical, except that analog changeover switches are provided on-card to enable the channel 1 error to be sent to all four hysteresis comparators to implement a single channel of multiple-hysteresis-band multilevel converter control. The analog switches also enable the channel 3 error to be sent to two hysteresis comparators to implement 2 pairs of channels of multiple hysteresis-band converter control.

The software and hardware functionality for this feature is not available with the default CPT-Mini2810 controller. Provision for the components exists on the CPT-Mini2810 artwork as supplied.

Please contact Creative Power Technologies to upgrade to the Hysteresis Controller version of the board.

1.8 Power Supply

The CPT-Mini2810 operates from +5V digital and +15V/-15V analog supplies via the MiniDSP plug-in compatible sockets.

2.0 Specifications

2.1 Plug-In Controller DSP Section

External Processor Card	CPT-DA2810 – with a Texas Instruments TMS320F2810 or 2811 DSP
On-card Memory	No on-card Memory – see the CPT-DA2810 Technical Manual for details
Clock	150MHz clock signal via **X7** to the CPLD (this link is soldered by default)
Reset	120ms hardware reset generated on the CPT-DA2810 from power up and supply failure. Triggered via **X10**.1 or by CPT-DA2810 on-card Link (**S1**)
Interrupts	Support for Gate Driver Faults, and 3 off external off-card interrupts

2.2 Mini Bus Interface

Mini Bus Description	8 data bits, 3 address bits, 3 I/O select lines, control signals (similar to Intel iSBX microbus)
Mini Bus I/O Address Space	24 I/O ports on Mini Bus, accessible as 3 banks of 8 addressable ports Generated within the CPLD from the SPI on the DA2810 interface
Connector – Plug-In	36 way IDC socket, **X14**

2.3 Analog Inputs

Number of A/D Inputs	16
Number of A/D Channels	12 off conditioned ADC signals to the CPT-DA2810 analog interface (**X2**)
Definition	Analog Switches select 4 of 8 analog channels. Individual switch selection between A and B channels 12 off single-ended input connections providing conditioned analog inputs
Input Voltage Range	±10V Maximum
Output Voltage Range	0-3V Maximum
Dynamic Response	Cut-off frequency >150kHz
Connector Input – Plug-In	26-way IDC Socket, **X2**, requiring ±15V analog supply, 16 off analog input signals, and AGND
Connector Output	Part of the CPT-DA2810 interface, **X8**

2.4 Analog Outputs

Definition	4 off 12-Bit Buffered DACs with output signal conditioning
Number of Channels	4
DAC Resolution	12 bits (1 x LSB = 4.88mV)
Voltage Range	$-\frac{2048}{2048}\times 10V = -10V$ to $\frac{2047}{2048}\times 10V = 9.995V$
Gain & Offset Adjustment	Software Calibration Required
DAC Settling Time	3 – 4.5µs
DAC Interface	Accessed via SPI interface with DAC1* (GPIOD6) chip select
Slew Rate	1.8V/µs
PCB Connection	10 pin shrouded IDC header, with output signals, and interleaved AGND (**X1**)

2.5 PWM Gate Drive Interface

Definition	A 16-way IDC connector, **X3**, providing 8 PWM outputs
PWM Outputs	8 PWM outputs consist of – a) EVA Mode (sourced from the CPT-DA2810 interface) 3 complementary pairs (6 outputs) with programmable deadband (0-102µs) 2 independent outputs generated by simple compare units ***or*** 1 complementary pair with programmable (CPLD generated) deadband b) Hysteresis Controller Mode (sourced from the CPLD and hysteresis hardware on-card) 4 complementary pairs (8 outputs) with programmable (CPLD generated) deadband
Gate Fault Interrupt	PDPINTA* on interrupt header, which when unmasked and active low, causes the timer compare outputs immediately to go to a high impedance state Pull-down resistors on the PWM outputs act to disable the PWM drive signals
Digital high output voltage threshold	3.30V
Digital low output voltage threshold	1.10V
Connector – Plug-In	16-way IDC socket, **X3**. GND also available on connector

2.6 Digital I/O

Definition	1 bank of 8 bit TTL digital input 1 bank of 8 bit TTL digital outputs (can be configured as PWM outputs) 1 bank of 6 bit TTL external interrupts. All four bits can be used as digital inputs
Digital high input voltage threshold	3.30V
Digital low input voltage threshold	1.10V
Digital outputs rated at	±35mA per bit, ABSOLUTE MAXIMUM
Typical digital high output voltage @ 10mA source	4.34V
Typical digital low output voltage @ 10mA sink	0.33V
Connector – Plug-In	20-way IDC socket, **X6**. +5V (DVCC) and GND also available on connector
Note: Output voltage specified for +5V DVCC	

2.7 Interrupts Interface

Definition	1 bank of 6 bit TTL external interrupts. These signals can also be configured as digital inputs
DSP Interrupts Available	PDPINTA* PDPINTB* XINT1A (interfaces to XINT1 via the CPLD) XINT2 CAP3 CAP6
External Reset	Off-card Reset signal (RESET_INPUT*) (normally high – active low to cause reset). Connected in parallel with reset switch, S1
Digital high input voltage threshold	3.30V
Digital low input voltage threshold	1.10V
Connector – Plug-In	16-way IDC socket, **X10**. GND also available on the connector

2.8 Communications Interface

Definition	The CPT-Mini2810 interface board has a TTL level serial port, a transmit control capable TTL serial port and a 4 wire clocked serial port.
Configuration	Serial Port SCIB is CPLD configurable to either a TTL level serial port (via the MiniDSP plug-in interface **X12**) or a TTL level serial port with a transmit control signal (**X13**) The 4 wire clocked serial port operates independently
Isolation	No

2.8.1 TTL Level Serial Interface

Definition	A 16-way IDC connector, **X12**, providing two-pin serial communications at a TTL level
Compatibility	Transmit is provided on **X12** pin 5 and Receive is provided on **X12** pin 3
Connector – Plug-In	16-way IDC socket, **X12**. GND also available on connector

2.8.2 TTL Level Serial Interface with Transmit Control

Definition	A 5-way molex connector, **X11**, providing two-pin serial communications at a TTL level with a separate transmit control. Capable of operation as an off-card RS-485 interface
Compatibility	The interface is compatible with the CPT-COM isolated battery powered RS-232 circuit board (pins 1-4) and the CPT-COM4 isolated RS-232/422/485 board
Configuration	Transmit Control Signal driven from TX_CTRL* (GPIOA15)
Connector – Plug-In	5-way molex header, **X11**. 3.3V and GND also available on connector

2.8.3 Clocked Serial Port Interface

Definition	A 10-way IDC connector, **X9**, providing 4 wire clocked serial communications port. +5V (DVCC) and GND made available on connector for external use
Compatibility	Buffered 4 wire I/O clocked serial communications protocol. Capable of operating in master or slave mode via M_S* (GPIOA14) signal.
Configuration	Off-card interface can be disabled through OC_SPI_EN (GPIOA13)
Connector – Plug-In	10-way IDC socket, **X9**. DVCC and GND also available on connector

2.9 Software

Support Software	Standard library source code, sample programs Texas Instruments: Code Composer Studio V3.1 and above

2.10 Power Supplies

Definition	The board's power supplies must be sourced from the plug-in sockets on the MiniDSP footprint
Input Voltage	Regulated +5VDC / GND - Digital Input Regulated +15V/-15V/AGND – Analog Inputs
Power Connector	Digital +5V Supply via Connectors **X6, X9** and **X14.** Analog +15V/-15V Supply via Connector **X2**

2.11 General

Physical Dimensions	L: 202mm
	W: 73mm
	H: 30mm approx.
Environmental	0 – 50°C Ambient operating temperature 5% - 95% non condensing humidity

3.0 Technical Details

3.1 Design Overview

The CPT-Mini2810 interface card is primarily designed to provide the core of a flexible inverter platform in conjunction with the CPT-DA2810. The CPT-DA2810 card is based around a Texas Instruments TMS320F2810 DSP chip, which has been designed for digital motor/motion control applications. On-card memory consists of 64k x 16 bit Flash and 18k x 16 bit RAM socket.

The CPT-Mini2810 card supports external communication through 1 off TTL serial port (selectable with transmit control) or a clocked serial peripheral interface. See section 3.3.4 for details.

For I/O expansion, the card has an I/O MINI BUS, which comprises 8 bi-directional data bits, 3 address lines, 3 decoded I/O select enable and normal bus read/write/control signals. The MINI BUS is electrically similar to Intel's iSBX bus. The MINI BUS connector on the CPT-Mini2810 card is designed to attach to a 36-way ribbon cable, allowing peripheral cards to be strung off 36-way headers as required. The MINI BUS is interfaced from the CPLD via 74LVX3245 level-shifting buffers. The DSP SPI interface is used to access the CPLD. See section 3.3.2 for details.

Power is supplied to the board via the plug-in connectors. The CPT-Mini2810 requires ±15V analog and +5V regulated supplies, see section 3.3.10.

3.1.1 Analog Inputs

The CPT-Mini2810 has 16 off analog inputs, and 12 of those inputs are available at the CPT-DA2810 interface at any given time. Eight of the analog inputs to the CPT-Mini2810 card are fed directly through buffers to the CPT-DA2810 interface, with the remaining 8 inputs fed through four dual analog switches to produce four signals to the CPT-DA2810 interface. The position of each analog switch is selected through the multiplexer interface. A buffered 2.5V reference is generated on card using the signal available from the CPT-DA2810 plug-in interface.

The TMS320F2810 DSP chip includes a single 12-bit Analog-to-Digital Conversion (ADC) module that is fed from one of two analog input banks. Each bank has its own sample and hold unit. The TMS320F2810 has a total of 16 analog input channels, with eight analog inputs provided to each bank through an 8-to-1 analog multiplexer. The maximum conversion time for each analog input bank is 80ns (with a 25MHz ADC clock). The ADC module can be set up to interleave the conversions between the two banks, effectively enabling one conversion to start before the previous one has been completed. This "pipelining" process enables the overall conversion time for "simultaneous" conversions to be reduced.

The analog channels on the CPT-Mini2810 card are designed to accept a ±10V analog input. Quad LF444 surface mount operational amplifiers have been used in all conditioning circuitry, since they have a low supply current. Each analog input signal is buffered with a unity-gain op-amp to provide a high impedance input. Each input then goes through a gain offset stage to condition the signals to 0-3V for entry into the ADC located on the CPT-DA2810.

Software compensation of any offsets should be done during calibration to compensate for component tolerance variations. The CPT-DA2810 board provides precision 1.25V and 2.5V analog reference voltages to four of the TMS320F2810 analog inputs (two per bank) to enable calibration of the offset and gain within each ADC bank. The analogs on the TMS320F2810 require calibration to ensure maximum performance and accuracy, as outlined in Texas Instruments document *spra989a.pdf*.

The ADC subsystem sample and holds can be synchronised to an external source through a TTL output. This output is shared with port B, bit 4 and must be configured correctly on the motherboard.

All unused analog inputs should be grounded.

3.1.2 Analog Outputs

There are two off quad 12-bit DACs (AD5624) on the CPT-Mini2810 circuit board. These DACs can be used for the on-card hysteresis controller (see *CPT-Mini2810 Hysteresis Controller Manual*) and one quad DAC (DAC1) is available for off-card use with ±10V signals. DAC1 contains four channels (DAC1A to DAC1D) whose outputs are buffered and an offset introduced to produce an approximate ±10V output range on connector **X1**. A digital input value of 0x0000 corresponds to -10V and a value of 0xFFF0 corresponds to $\frac{2047}{2048} \times 10V = 9.995V$.

The output value of each DAC is set via the SPI interface from the CPT-DA2810. There are separate chip select lines (DAC1* and DAC2*) on the CPT-DA2810 interface connector.

The Analog Output 10-way IDC connector contains the four DAC output signals and interleaved grounds.

3.1.3 Digital Inputs

The CPT-Mini2810 card supports two independent sources for TTL digital inputs, comprising an 8-bit fully buffered bank, and a 6-bit digital input port which can be used as general purpose digital input or for external interrupts.

The buffered TTL logic level inputs are provided through a shared 20-way IDC header (Pins 9-16). This header is shared with the TTL logic level digital outputs (section 3.1.4). The header supplies the 16 signals as well as ground and +5V supplies on pins 17-20.

The 6-bit TTL logic level inputs are fully buffered and are accessed via a 16-way IDC header. The port is normally available for use as external interrupts. All six pins can be redefined as general digital inputs. This port also provides for an external reset signal input.

3.1.4 Digital Outputs

The CPT-Mini2810 card contains 8 digital output bits, which have been configured into one latched bank of 8 bits.

The buffered TTL logic level outputs are provided through a 20-way IDC header (Pins 1-8). This header is shared with the TTL logic level digital inputs (section 3.1.3). The header supplies the 16 signals as well as ground and +5V supplies on pins 17-20.

3.1.5 PWM Signals

The PWM interface uses a 16-way IDC header, **X3**, to connect to external gate drive interface circuitry. This interface enables the CPT-Mini2810 to support 4-arm bridge operation, as the PWM header outputs 8 buffered PWM signals.

A general fault trip signal is provided as a fast fault indicator to the TMS320F2810 DSP. This signal connects to the PDPINTA* interrupt on the DSP and is sourced from PDPINTA* on **X10.** When triggered by a fault, it causes all PWM outputs to be placed into a low state. A pull-down resistor pack on the DSP's PWM pins is used to fully disable the PWM outputs when this fault trip occurs. Ground signals are interleaved with the PWM outputs on the header, to reduce noise.

The source of the PWM signals can be selected to be either the CPT-DA2810 interface (Event Manager A – EVA) or the on-card hysteresis controller. This functionality is not available on the base CPT-Mini2810 CPLD programming. Please contact Creative Power Technologies for the Hysteresis Controller upgrade.

The digital outputs on the Digital I/O connector can be configured to operate as PWM signals sourced from Event Manager B on the CPT-DA2810 interface. This provides 8 off buffered PWM signals on connector **X6** and the corresponding interrupt PDPINTB* is on connector **X10**.

The Event Manager PWM outputs are disabled by default within the CPLD to ensure that they start up in an OFF condition. They must be explicitly enabled before switching can commence.

3.1.6 On-card Power Supplies

The CPT-Mini2810 requires the following power supplies

- regulated +/-15V/AGND supplies provided on the analog connector, **X2**.
- regulated +5V/GND supply provided on connectors, **X6**, **X9** and **X14.**

3.2 Installation and Setup

3.2.1 General

The CPT-Mini2810 interface card is supplied with the CPT-DA2810 DSP controller and configured with a Debugging Monitor program and Boot-Loader, basic VSI software and a programmed CPLD.

The card must be provided with power (+/-15V/AGND and +5V/GND) via the plug-in sockets

All necessary links are included and installed onto the card before delivery. Standard software is loaded into the on-chip FLASH memory.

The standard software supplied with the CPT-DA2810 card uses an RS-232 serial terminal as the system console through SCIA, which is located on the CPT-DA2810 (connector **X3**).

The CPT-DA2810 card uses many of the features of the TMS320F2810 DSP chip. A complete description of this processor is provided in the *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811 and TMS320C2812 Digital Signal Processors Data Manual* available from the Texas Instruments website. Document Number *SPRS174O*.

There are multiple documents available within the TMS320F2810 literature that focus on the individual sections within the DSP chip.

Consult the TI Website: http://focus.ti.com/docs/prod/folders/print/tms320f2810.html for the complete list of available documentation on the TMS320F2810 DSP.

Please also refer to the *CPT-DA2810 Technical Manual*.

3.2.2 Option Links

There are no option links on the CPT-Mini2810 Interface Card. All board options are configured within the CPLD.

3.2.3 External Connectors

CONNECTOR DESIGNATOR	DESCRIPTION	TYPE	SECTION
X1	Analog Outputs	IDC Header	3.3.7
X2	Analog Inputs	IDC Socket	3.3.6
X3	PWM	IDC Socket	3.3.9
X4	Hysteresis Controller outputs	MASCON	
X5	Hysteresis Controller inputs	MASCON	
X6	Digital I/O	IDC Socket	3.3.7
X7	CPT-DA2810 – CLKOUT Interface	Wire Link	3.3.1
X8	CPT-DA2810 Plug-in	IDC Socket	3.3.1
X9	Clocked Serial Port	IDC	3.3.5
X10	External Interrupt Inputs	IDC	3.3.7
X11	TTL Serial Communications (with Transmit Control)	MASCON	3.3.4.2
X12	TTL Serial Communications	IDC Socket	3.3.4.1
X13	CPLD JTAG	IDC Header	
X14	Mini BUS	IDC Socket	3.3.3

Table 3-1: Off-card Connector Definitions

Note: IDC = IDC Header

3.3 Card Options and Connector Descriptions

The CPT-Mini2810 is designed to mount directly onto a custom-designed motherboard, such as the CS-IIB, without the need for ribbon cable connections and, in conjunction with the CPT-DA2810, acts as a drop-in upgrade for the CS-MiniDSP, also available from Creative Power Technologies.

The following sections describe the configuration and operation of sections on the CPT-Mini2810 board.

3.3.1 CPT-DA2810 Plug-In Connector

The interface between the CPT-Mini2810 and the CPT-DA2810 is the 80 way dual-in-line connector, **X8**. The detailed pinout description is given in Appendix D and shown in Figure 3-1 and Figure 3-2.

Note that the CPT-Mini2810 does not use all of the pins indicated within Figure 3-1 and Figure 3-2, or their associated peripheral modes. Please refer to either the relevant sections of this manual to determine which peripheral modes are supported or Appendix D.

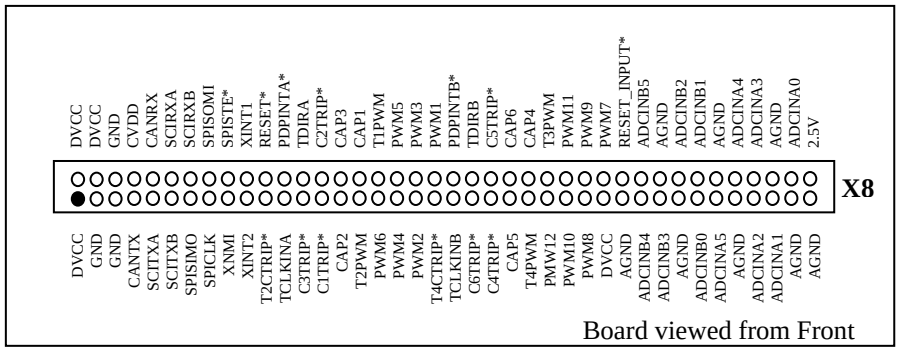


Figure 3-1: CPT-DA2810 Plug-in Connector – "Peripheral I/O" definitions (X8)

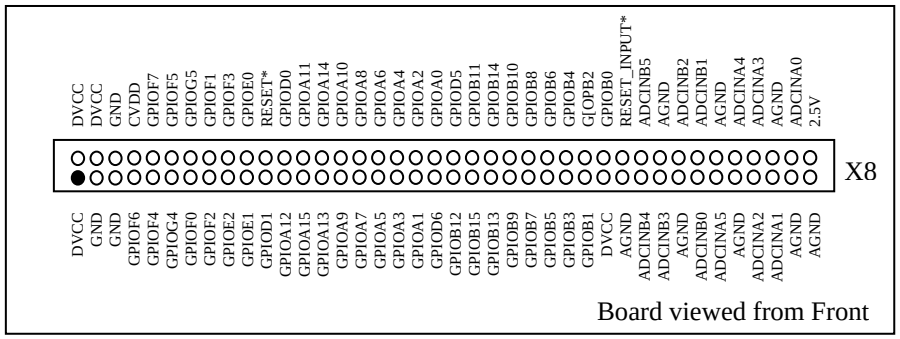


Figure 3-2: CPT-DA2810 Plug-in Connector – GPIO definitions (X8)

There is also a synchronising CLKOUT signal that is provided from the CPT-DA2810 to the CPT-Mini2810 board for use by the CPLD. This signal is passed down to the CPT-Mini2810 via the soldered connection **X7**.

3.3.2 On-Card CPLD

The CPT-Mini2810 has an Altera MAX II EPM570T100C5N CPLD that has been programmed to perform several functions. The CPLD has static memory and is supplied with a base level program that enables core CS-MiniDSP functionality to be maintained. There are expansion programs available from Creative Power Technologies, if additional CPLD functionality is required (eg. hysteresis controller).

The CPLD is accessed from the CPT-DA2810 interface via the SPI in Master Mode. The CPLD is programmed to perform the following functions:

- SPI to Mini Bus interface (see 3.3.3)
- Serial Port B Receiver Selection
- Hysteresis Analog Input Selection
- Interrupt XINT1 Source Selection
- EVA Source Configuration
- EVA Simple Compare Deadband Generation
- EVB Simple Compare Source Configuration
- EVB Simple Compare Deadband Generation

In addition, two pins on the CPT-DA2810 interface, GPIOD1 and GPIOF7, are available for direct bit accessing of the CPLD. These pins are defined as outputs from the CPLD by default.

The CPLD is enabled by asserting the CPLD_CS* line LOW and clocking 3 bytes to the SPI interface with the format as described below.

The first byte, BYTE 0 provides the CPLD address information

For a write command:

- BYTE 1, provides the data to be written,
- BYTE 2, is a dummy data.

Table 3-2 and Table 3-3 show the structure of the address and data bytes for a write command

For a read command:

- BYTE 1 is dummy data
- BYTE 2 is the data back from the specified address.

Table 3-4 and Table 3-5 show the structure of the address and data bytes for a write command

BYTE 0								**BYTE 1**								**BYTE 2**							
MSB																							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCS1	SCS0	SMA4	SMA3	SMA2	SMA1	SMA0	R/W*	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X	X

Table 3-2: SPI CPLD Write Data Definition

BYTE	BIT(S)	NAME	DESCRIPTION
0	23 – 22	SCS1 – SCS0	Chip Select 00 Mini Bus address range CS0* 01 Mini Bus address range CS1* 10 Mini Bus address range CS2* 11 Additional CPLD Peripherals/Registers
	21 – 17	SMA4 – SMA0	Memory Address within the Chip Select Ranges
	16	R/W*	Read / Write* signal – decoded to separate CPLD outputs **0 Write mode (WR* = 0, RD* = 1)** 1 Read mode (WR* = 1, RD* = 0)
1	15 – 8	D7 – D0	Data Lines
2	7 – 0	X	Don't Care

Table 3-3: SPI Bit Allocation for CPLD Write Access

BYTE 0								BYTE 1								BYTE 2							
MSB																							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCS1	SCS0	SMA4	SMA3	SMA2	SMA1	SMA0	R/W*	X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

Table 3-4: SPI CPLD Read Data Definition

BYTE	BIT(S)	NAME	DESCRIPTION
0	23 – 22	SCS1 – SCS0	Chip Select 00 Mini Bus address range CS0* 01 Mini Bus address range CS1* 10 Mini Bus address range CS2* 11 Additional CPLD Peripherals/Registers
	21 – 17	SMA4 – SMA0	Memory Address within the Chip Select Ranges
	16	R/W*	Read / Write* signal – decoded to separate CPLD outputs 0 Write mode (WR* = 0, RD* = 1) **1 Read mode (WR* = 1, RD* = 0)**
1	15-8	X	Don't Card
2	7 – 0	D7 – D0	Data Lines – Read Data

Table 3-5: SPI Bit Allocation for CPLD Read Access

The data registers and ports within the CPLD are all accessed via the SPI interface using the data structures described above. The complete list of valid peripheral addresses and registers is given in Table 3-6. Please refer to the section indicated in the table for further detailed descriptions on the peripherals and their registers.

Function	*Register*	*SPI Address*	*Section*
Mini Bus– Address Range		0x00 – 0x8F	3.3.3
Serial Communications Interface B Mode Select	SCIBMODE	0xC2	3.3.4
Capture Port Mode Select	CAPQEP	0xC4	3.3.8.2
Interrupt XINT1 Select	INTSEL	0xC6	3.3.8.1
EVA Command Configuration	EVACOMCON	0xD0	3.3.9
EVA Deadband Generator	EVACONDB	0xD2	3.3.9
EVB Command Configuration	EVBCOMCON	0xD4	3.3.9.1
EVB Deadband Generator	EVBCONDB	0xD6	3.3.9.2
Analog Switch Selection	ANLGSW	0xD8	3.3.10[1]
GPIO D1 and F7	GPIO	0xDA	3.3.11
Date of CPLD Compilation	DATELO/DATEHI	0xFA/0xFC	3.3.12
CPLD Version Number	VERSION	0xFE	3.3.12
Special (User) Function Register	SPECIAL	0xF0	3.3.13

Table 3-6: SPI CPLD Peripheral Address Mapping

[1] This definition is available within the *CPT-Mini2810 Hysteresis Controller Technical Manual* available separately from Creative Power Technologies.

3.3.3 Mini Bus I/O Interface

The 36 way I/O bus on the CPT-Mini2810 card provides an expansion capability for a variety of standard and custom peripherals to interface to the board. The Mini Bus consists of an 8 bit bi-directional data bus, three address lines, three decoded chip select line and normal processor bus control signals such as RD*, WR*, INT*, etc as shown in Figure 3-3. The Mini Bus is electrically similar to Intel's iSBX microbus. The signals available on the Mini Bus are shown in Figure 3-4.

The Mini Bus is designed to allow both rapid prototype development of peripheral devices, and to allow more substantial expansion, using a range of standard peripheral cards.

For prototype development, no off-card decoding is normally required. The decoded bus chip select lines (CS0*, CS1* and CS2*) allow up to three peripheral devices to be directly selected (within defined address ranges) without further componentry. The addressing for the Mini Bus interface is shown in Table 3-7.

The TTL level signals are fully buffered (74LVX3245), with the buffer providing level translation between the 3.3V CPT-Mini2810 core and the external 5V Mini Bus interface. The CPT-Mini2810 Mini Bus connector, **X14**, is a 36-way bottom loaded socket.

The TMS320F2810/TMS320F2811 DSPs do not have an external data/address bus. Therefore the parallel Mini Bus on the CPT-Mini2810 board is created from the synchronous (clocked) serial interface (SPI) within the MAX II EPM570T100C5N CPLD.

The address range for the SPI Mini Bus interface is 0x00 to 0x8F. The specific decoding is given in Table 3-7.

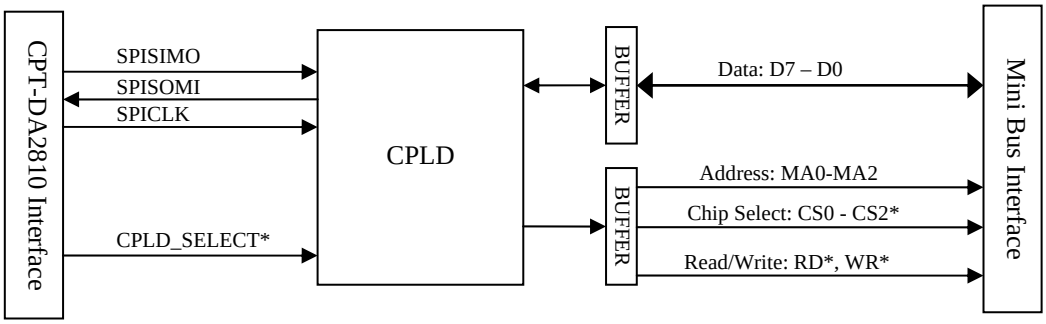


Figure 3-3: SPI to Mini Bus Interface

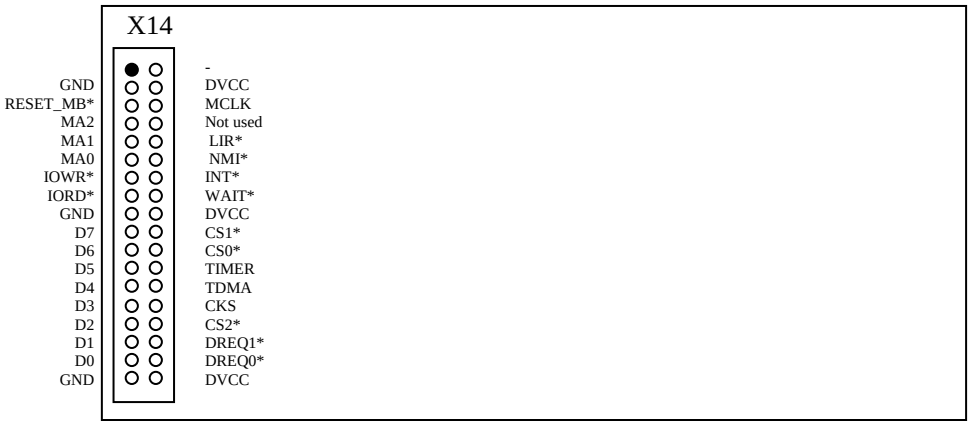


Figure 3-4: Mini Bus I/O Connector (X14)

The CPLD decodes the address (BYTE 0) from the SPI into:

- an active chip select (assert low one only of CS2* – CS0*),
- the specific address within that address range (MA2-MA0) and
- A read or write (by asserting low either WR* or RD*).

- The 8 bit data bus (D7 – D0) is located in BYTE 1 for a write and BYTE 2 for a read. This transfers data to or from the specified address.

For a write: Once the address has been established, and the data set up, the MINIBUS* and WR* signals are asserted low to enable the buffer in output mode to write the data (D7-D0) to the bus

For a read: Once the address has been established, the MINIBUS* signal is asserted low with the RD* signal and the data read back from the bus

BYTE	BIT(S)	NAME	DESCRIPTION
0	23 – 22	SCS1 – SCS0	Chip Select 00 CS0* (assert CPLD output pin LOW) 01 CS1* (assert CPLD output pin LOW) 10 CS2* (assert CPLD output pin LOW)
	21 – 20	SMA4 – SMA3	00
	19 – 17	SMA2 – SMA0	Memory Address within the Chip Select Range Maps directly to CPLD outputs MA2 – MA0
	16	R/W*	Read / Write* signal – decoded to separate CPLD outputs 0 Write mode (WR* = 0, RD* = 1) 1 Read mode (WR* = 1, RD* = 0)
1	15 – 8	D7 – D0 X	Data Lines (WRITE MODE) - decoded to/from CPLD data output pins D7 – D0 Dummy Bits (READ MODE)
2	7 – 0	X D7 – D0	Dummy Bits (WRITE MODE) Data Lines (READ MODE) - decoded to/from CPLD data output pins D7 – D0

Table 3-7: SPI Mini Bus Address Decoding

3.3.3.1 Mini Bus Master / Slave Mode

The Mini Bus interface on the CPT-Mini2810 is configurable as a peripheral on another card's mini bus, which enables it to act as a slave device. When used in this mode the address of the peripheral must be set to ensure that an externally initiated Mini Bus read/write is recognised.

The default programming of the CPLD only supports configuration in master mode. Please contact Creative Power Technologies to upgrade to the CPLD programming that supports Master/Slave mode.

3.3.4 Communications

The CPT-Mini2810 has one asynchronous port (SCIB) and one synchronous serial port (SPI). Asynchronous serial port B can be configured in one of two modes on the board.

The available serial port options on the CPT-Mini2810 are:

- 1 off TTL level Serial Communications Interface (SCIB-TTL – **X12**)
- 1 off TTL level Serial Communications Interface with transmit control (SCIB-485 – **X11**)
- 1 off Clocked Serial Peripheral Interface (SPI – **X9**)

The on-card TTL level Serial Communications Interface B source can be selected by writing to the CPLD SCIBMODE register (Address: 0xC2). The data byte, Byte 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
SPD	X	X	X	X	X	X	SC

Table 3-8: SCIBMODE Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	SPD	Internal Bidirectional SPI Switch enable (Special Function CPLD required) 0 Standard operating mode
	6 – 1	Reserved	
	0	SC	Serial Port B receive signal (SCIRXB) sourced from: 0 TTL – Plug-in TTL level Connector 1 485 – RS-485 Molex Connector

Table 3-9: SPI Bit allocation for SCIBMODE register

Caution: Do not set bit SPD to 1 if a Special Function CPLD is not present. This has the effect of disabling the SPI interface and requires either a cold restart or a special instruction via the GPIO bits to return it to the standard operating mode.

The CPLD can be modified with a user specific program. The SPD bit is designed to enable that user program to be accessed and enabled. However, this will disable the basic CPLD registers SPI operation until the CPLD is returned to the standard mode. This is achieved through the GPIO bits, but is not covered in this basic manual. Users are strongly advised to not set the SPD bit.

On power up the connection defaults to the TTL level Serial Communications Interface SCIB-TTL.

The TMS320F2810 DSP supports communication through two asynchronous serial ports and two synchronous serial ports. SCIA is available ONLY on the CPT-DA2810 board (**X3**) and the second synchronous serial port (MCBSP) is used on the CPT-DA2810 for the 1Mb Flash ROM.

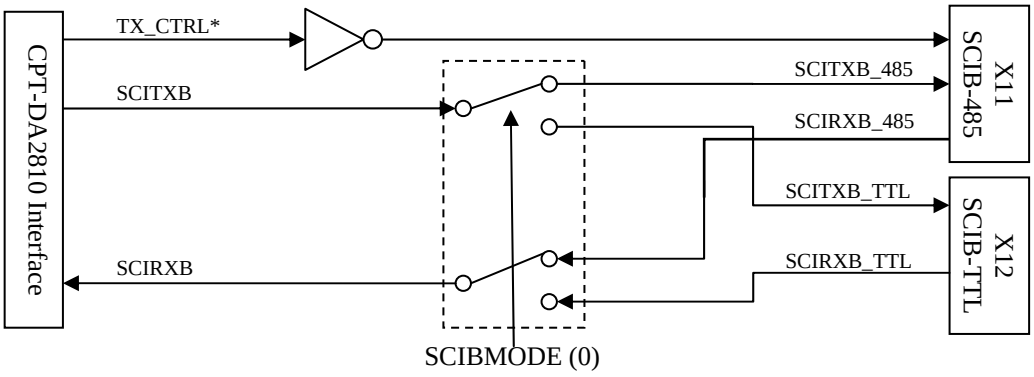


Figure 3-5: SCIB Configuration

3.3.4.1 TTL-Level Serial Port

SCIB can be configured as a TTL-level communications port (connector **X12)** by writing 0x00 to the SCIBMODE register. This provides compatibility with the CS-MiniDSP peripherals. The active pins on connector **X12** are given in Figure 3-6. There are no changeover links available on the board for the Rx/Tx signals on this connector.

The serial port signals are provided off-card at TTL levels. The motherboard can provide optional isolation for the serial interface as well as conversion to alternative communications protocols – RS-232.

The transmit signal, SCITXB, is provided at 3.3V TTL level and the receive signal, SCIRXB_TTL, is TTL level compatible. Both signals are buffered on-card.

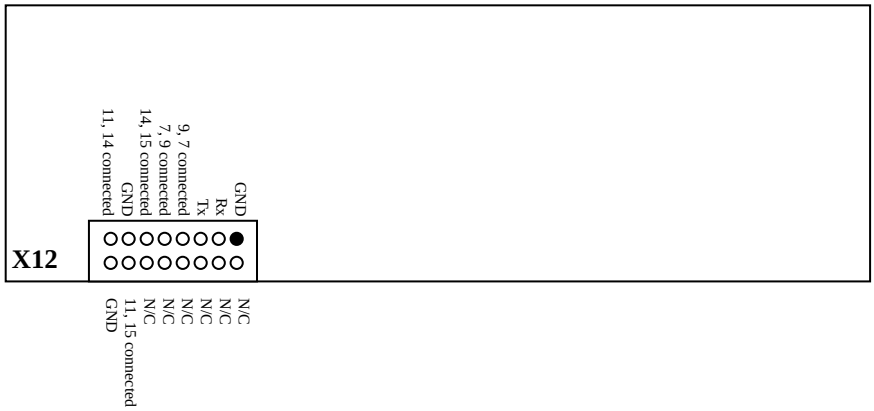


Figure 3-6: Signal Pins for TTL Level Communications Protocol (X12)

3.3.4.2 TTL-Level Serial Port with Transmit Control

SCIB can be configured to TTL-level RS-485 compatible communications mode (connector **X11)** by writing 0x01 to the SCIBMODE register. The SCIRXB-485 receive line is set as active to the CPT-DA2810 interface SCIRXB pin. A Transmit Control pin is available on the molex header if RS-422/485 communications is required off card. The CPT-DA2810 uses TX_CTRL* for this signal.

All level shifting, terminating resistors and isolation for this interface should be located on the off-card peripherals. This interface is only available at TTL level on a 5-pin Molex connector, **X11**, that contains a digital ground, 3.3V power supply and the three signals, as shown in Figure 3-7.

Note that the pinouts on this connector are compatible with the CPT-COMx range of isolated interface boards available from Creative Power Technologies.

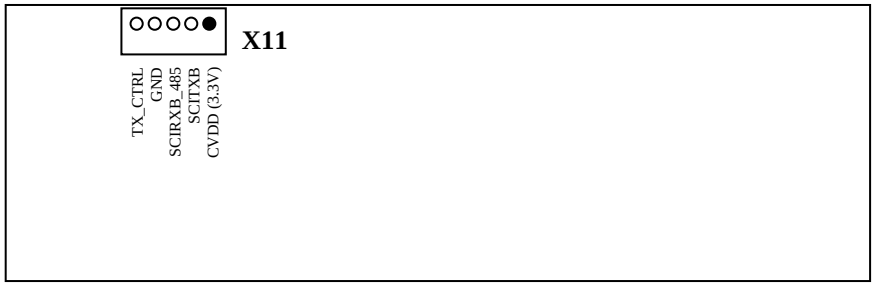


Figure 3-7: Pinouts for COM B RS-485 Serial Port (X11)

3.3.5 Clocked Serial Peripheral Interface

The clocked serial peripheral interface on the CPT-Mini2810 supports a master/many slave configuration for communication between multiple SPI peripherals. The interface consists of transmit and receive, a serial clock and an enable signal. The interface also provides a +5V (DVCC) and GND signal on the connector. A 10-way IDC socket, **X9**, is used for this interface, with the pinouts listed in Figure 3-8.

The SPI can be software configured to operate in either Master or Slave mode. When configured in master mode, the CPT-Mini2810 sends out the synchronising serial clock signal to the slave devices. In slave mode the CPT-Mini2810 monitors the slave receive, enable and SCLK lines for transmitted data requests.

There are 4 peripherals connected to the SPI port from the CPT-DA2810 interface on the CPT-Mini2810 board.

- CPLD (EPM570T100C5N) – Master Mode only
- 2 off quad DACs (AD5624RBRMZ-5) – Master Mode only
- 1 off Master/Slave connection to the plug-in connector (as shown in Figure 3-8)

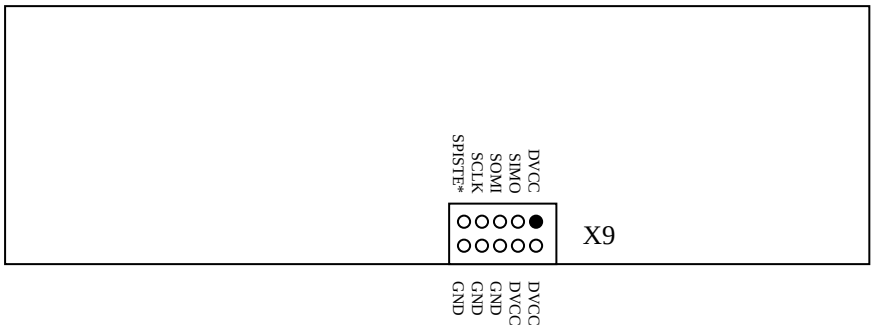


Figure 3-8: Clocked Serial Port Interface (X9)

The CPT-DA2810 interface has separate chip selects for each peripheral on the SPI interface, as given in Table 3-10 below.

Peripheral Name	*Schematic Chip Select Signal Name*	*CPT-DA2810 Interface*		*TMS320F2810*	*SPI Mode*
		Pin	*Name*	*DSP Pin*	
DAC1	DAC1*	40	GPIOD6	61	Master
DAC2	DAC2*	46	GPIOB13	46	Master
CPLD	CPLD_CS*	8	GPIOF6	64	Master
Off-card SPI peripherals	SPISTE*	16	SPISTE*	28	Master/Slave
	OC_SPI_EN*	28	GPIOA13	89	Enable Off-card SPI

Table 3-10: SPI Peripherals Chip Select Definitions

Note: When the SPI is configured in slave mode the CPT-Mini2810 peripherals are not accessible from the on-card CPT-DA2810. Careful consideration must be made to the timing within any user programs to ensure all required peripherals are still able to function correctly when the slave mode is incorporated.

3.3.5.1 Off-card SPI Access

The off-card SPI can be configured in either Master or Slave mode for interaction with external SPI devices, or a second CPT-Mini2810/CPT-DA2810. The SPI mode is selected by asserting M_S*(GPIOD1) HIGH for master, or LOW for slave mode.

If the off-card SPI is configured in slave mode the user must disable the off-card SPI buffers (OC_SPI_EN*) before switching to on-card master mode to communicate with any on-card peripherals. This is required to prevent a bus contention between an off-card master and the on-card peripheral communication. The level translation buffers can be tri-stated by driving the OC_SPI_EN* (GPIOA13) pin high, which puts the SPI buffer voltage regulator into a shutdown mode.

3.3.6 Analog Inputs

The 16 analog inputs on the CPT-Mini2810 analog input connector must feed into 12 off analog conditioning channels that are available on the CPT-DA2810 interface. Eight of the inputs are direct fed to the CPT-DA2810 interface with the input to the remaining four channels selected through four dual analog switches, as shown in Figure 3-9. This configuration ensures compatibility with the existing CS-MiniDSP analog input interface.

Each analog channel accepts a maximum ±10V input and is conditioned on-card to 0-3Vdc. The CPT-DA2810 board provides a low pass glitch filter and protection diodes.

All unused analog inputs should be grounded.

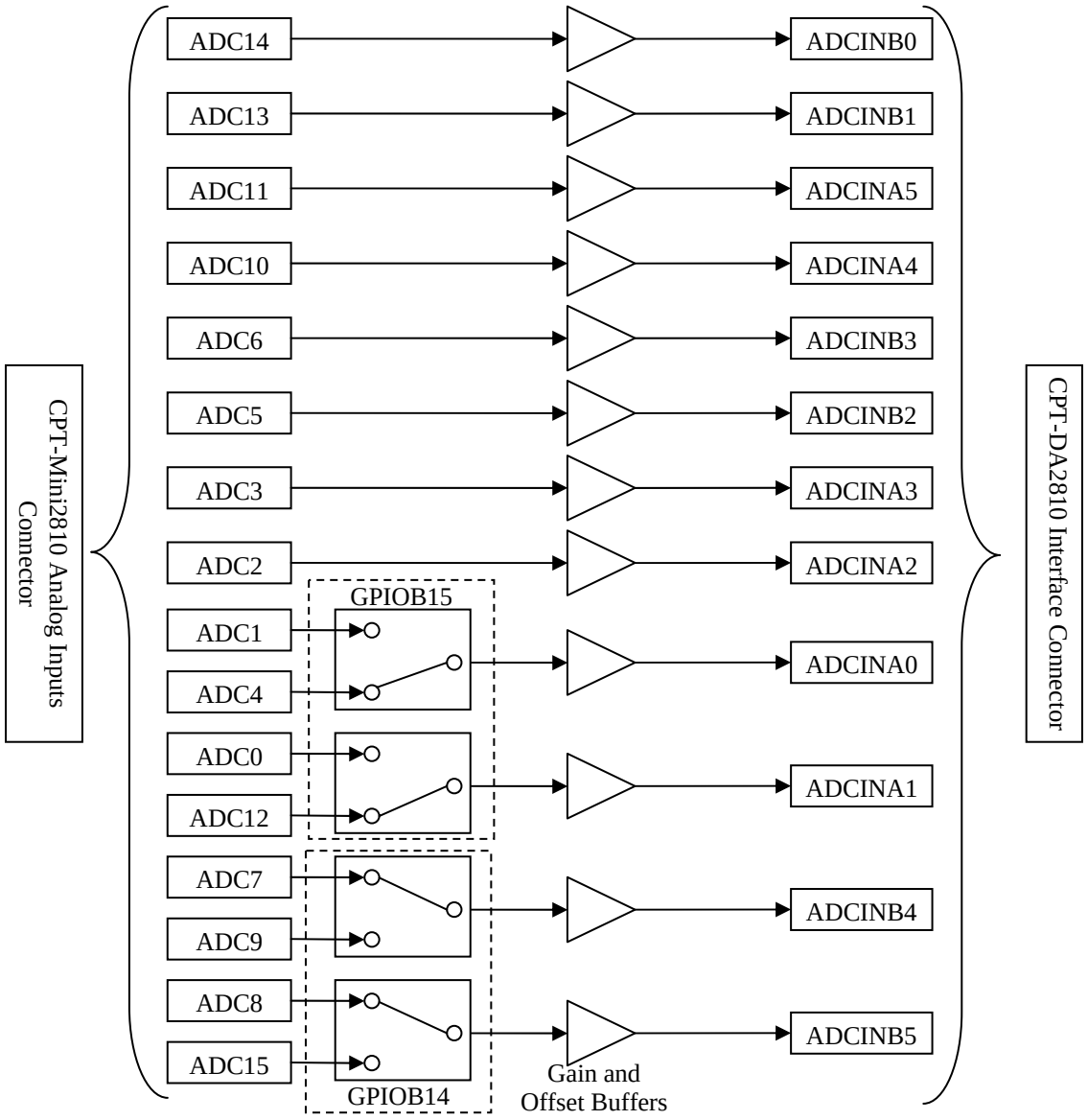


Figure 3-9: Mapping of Analog Inputs to CPT-DA2810 Interface

The analog signals come onto the board via a 26-way IDC socket, **X2**, Figure 3-10.

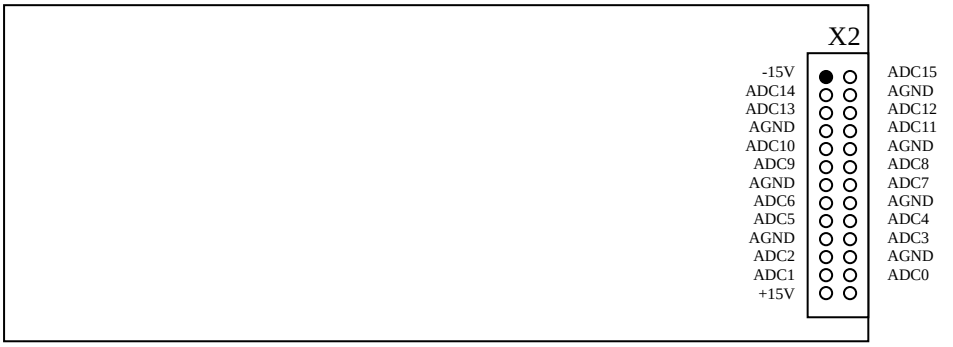


Figure 3-10: Pinouts for Analog Input Connector (X2)

The active inputs for the shared analog input channels are selected from the CPT-DA2810 interface bits GPIOB14 and GPIOB15 as shown in Table 3-11. The MiniDSP Input Analogs Interface maps to the CPT-DA2810 analog channels as shown in Table 3-12.

BIT(S)	NAME	DESCRIPTION
GPIOB15	SW_A	Switch Selection for ADCINA0 and ADCINA1 channels See Table 3-12 for address decoding
GPIOB14	SW_B	Switch Selection for ADCINB4 and ADCINB5 channels See Table 3-12 for address decoding

Table 3-11: DSP Bit allocation for Analog Switch Selection

SW_A	SW_B	MINIDSP INTERFACE INPUT ANALOG CHANNEL	CPT-DA2810 ANALOG CHANNEL
0	X	ADC4	ADCINA0
		ADC12	ADCINA1
1	X	ADC1	ADCINA0
		ADC0	ADCINA1
X	0	ADC7	ADCINB4
		ADC8	ADCINB5
X	1	ADC9	ADCINB4
		ADC15	ADCINB5

Table 3-12: Decoded Analog Input Channel Selection

Table 3-13 shows the mapping between the analog input signals on connector, **X2**, their corresponding ADC designators, channels and the pin on the CPT-DA2810 DSP.

CONNECTOR X2, PIN	ANALOG INPUT	DSP ADC CHANNEL	CONNECTOR X8, PIN	CPT-DA2810 DSP PIN
2	ADC15 [2 SW_B=1]	ADCINB5	61	7
3	ADC14	ADCINB0	68	2
5	ADC13	ADCINB1	67	3
6	ADC12 [3 SW_A=0]	ADCINA1	71	125
8	ADC11	ADCINA5	77	121
9	ADC10	ADCINA4	76	122
11	ADC9 [4 SW_B=1]	ADCINB4	62	6
12	ADC8 [2 SW_B=0]	ADCINB5	61	7
14	ADC7 [4 SW_B=0]	ADCINB4	62	6
15	ADC6	ADCINB3	64	5
17	ADC5	ADCINB2	65	4
18	ADC4 [5 SW_A=0]	ADCINA0	70	126
20	ADC3	ADCINA3	74	123
21	ADC2	ADCINA2	73	124
23	ADC1 [5 SW_A=1]	ADCINA0	70	126
24	ADC0 [3 SW_A=1]	ADCINA1	71	125

Table 3-13: Analog Input Mappings

The CPT-Mini2810 requires regulated ±15V on connector, **X2** (+15V on pin 25 and –15V on pin 1).

[2] DSP Channel ADCINB5 is shared between ADC8 & ADC15 analog inputs
[3] DSP Channel ADCINA1 is shared between ADC12 & ADC0 analog inputs
[4] DSP Channel ADCINB4 is shared between ADC7 & ADC9 analog inputs
[5] DSP Channel ADCINA0 is shared between ADC4 & ADC1 analog inputs

Note: The selection of the analog channels and the error summing junctions for the hysteresis controller are covered in the *CPT-Mini2810 Hysteresis Controller Manual.*

The mapping of analog inputs between the CPT-Mini2810/DA2810 and the available peripheral boards (CS-GIIB, CS-IIB and CS-IIC) are given in Table 3-14

ANALOG INPUT	DSP ADC CHANNEL	CS-GIIB	CS-IIB	CS-IIC
ADC15	ADCINB5 [2 SW_B=1]	Vgen	Vac6	Vac6
ADC14	ADCINB0	Vdc2	Vac5	Vac5
ADC13	ADCINB1	I5	I5	I5
ADC12	ADCINA1 [3 SW_A=0]	Vac3	Vac3	Vac3
ADC11	ADCINA5	Vac2	Vac2	Vac2
ADC10	ADCINA4	I2	I2	I2
ADC9	ADCINB4 [4 SW_B=1]	APOT2	APOT2	APOT2
ADC8	ADCINB5 [2 SW_B=0]	Vdc4	Vdc2	Vdc2
ADC7	ADCINB4 [4 SW_B=0]	I6	I6	I6
ADC6	ADCINB3	Vdc1	Vac4	Vac4
ADC5	ADCINB2	I4	I4	I4
ADC4	ADCINA0 [5 SW_A=0]	I3	I3	I3
ADC3	ADCINA3	Vac1	Vac1	Vac1
ADC2	ADCINA2	I1	I1	I1
ADC1	ADCINA0 [5 SW_A=1]	APOT1	APOT1	APOT1
ADC0	ADCINA1 [3 SW_A=1]	Vdc3	Vdc1	Vdc1

Table 3-14: Peripheral Board Analog Mappings

3.3.7 DAC Voltage Outputs

There are two off quad 12-bit DACs on the CPT-Mini2810 circuit board. DAC outputs 1-4 are available externally on connector **X1** see Figure 3-11., whilst both DACs are used as part of the hysteresis controller functionality to set up the reference waveforms.

The four external DAC voltage outputs are configured to provide a bipolar ±10V output from a AD5624RBRMZ-5 quad channel 12-bit DAC. The output voltage is software adjustable via the port definitions as given in Table 3-15 to Table 3-18. The DAC output is available on a 10-way IDC header, **X1**. Refer to the AD5624 datasheet for full programming details.

The DACs are accessed from the CPT-DA2810 interface via the SPI in Master Mode.

The external DAC is enabled by asserting the DAC1* line LOW and clocking 3 bytes to the SPI interface with the structure given in Table 3-15. The DAC has a 24 bit wide shift register with the following format

The first two bits are don't care bits. The next three bits are the Command bits, C2 to C0 (see Table 3-17), followed by the 3-bit DAC address, A2 to A0 (see Table 3-18), and then the 12-bit data-word. The data-word comprises the 12- bit input code followed by 4 don't care bits, see Table 3-15. These data bits are transferred to the DAC register on the 24th falling edge of SCLK.

BYTE 0								BYTE 1								BYTE 2							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

Table 3-15: DAC SPI Access Structure

BIT(S)	NAME	DESCRIPTION
23 – 22		Don't Care
21 – 19	C2 – C0	Command Definition
18 – 16	A2 – A0	Address Command
15 – 4	D11 – D0	
3 – 0		Don't Care

Table 3-16: SPI Bit allocation for DAC access

COMMAND	C2	C1	C0
Write to input register *n*	0	0	0
Update DAC register *n*	0	0	1
Write to input register *n*, update all (software LDAC)	0	1	0
Write to and update DAC channel *n*	0	1	1
Power down DAC (power-up)	1	0	0
Reset	1	0	1
Load LDAC register	1	1	0
Reserved	1	1	1

Table 3-17: DAC Command Definition

ADDRESS	A2	A1	A0
DAC A	0	0	0
DAC B	0	0	1
DAC C	0	1	0
DAC D	0	1	1
All DACs	1	1	1

Table 3-18: DAC Address Definition

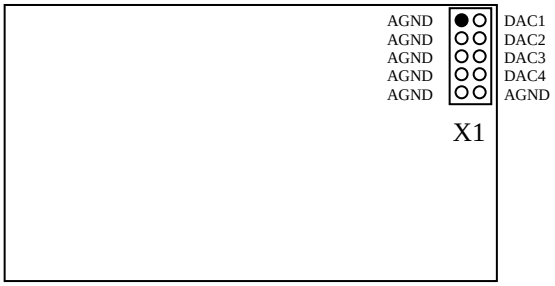


Figure 3-11: DAC Voltage Output Connector (X1)

3.3.8 Digital I/O Connectors

The Digital I/O bank is externally interfaced through a 20-pin IDC socket connector **X6**. Pinouts for connector **X6** are shown in Figure 3-12. Each bank is preconfigured as a digital output (**X6** pins 1-8) or digital input (**X6** pins 9-16). The TTL level signals are fully buffered (74LVX3245), with the buffer providing the level translation between the 3.3V core on the CPT-Mini2810 and the external 5V interface.

The digital input bank has 4 bits that are fed directly to the CPT-DA2810 connector, and 4 bits that are fed to the CPLD with the status of the CAPQEP register determining their destination on the CPT-DA2810 connector. The available options for these bits are given in Table 3-19. If unused this port should have pull down resistors added to it to prevent the inputs from floating (connection on X6 pins 9 to 16 to pin 18/20).

The digital output bank has 6 bits that are fed directly from the CPT-DA2810 connector, and 2 bits that are fed from the CPLD with their source selected by the status of the EVBCOMCON and EVBCONDB registers. The available options for these bits are shown in Table 3-19.

Standard library functions are available for reading and writing to these memory addresses and to set the CPLD mappings.

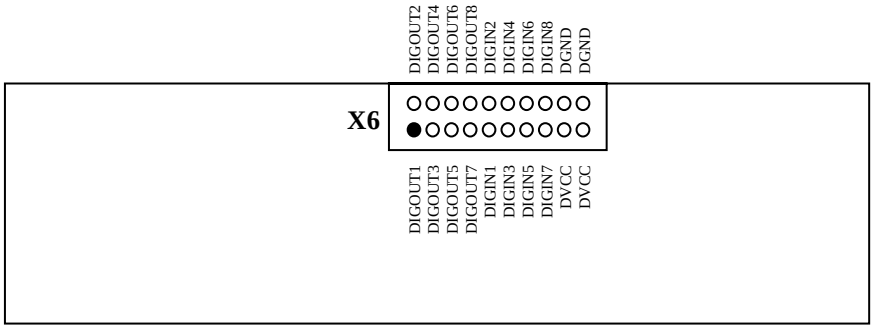


Figure 3-12: I/O Bank Connector (X6)

The mapping of the digital I/O port to the CPT-DA2810 interface is given in Table 3-19.

CONNECTOR X6, PIN	DIGITAL I/O SIGNAL	DSP PORT DEFINITION	CONNECTOR X8, PIN	CPT-DA2810 DSP PIN
1	DIGOUT1	GPIOB0	57	33
2	DIGOUT2	GPIOB1	56	34
3	DIGOUT3	GPIOB2	55	35
4	DIGOUT4	GPIOB3	54	36
5	DIGOUT5	GPIOB4	53	37
6	DIGOUT6	GPIOB5	52	38
7	DIGOUT7	See Digital Output Selection 3.3.9.2		
8	DIGOUT8			
9	DIGIN1	GPIOB11	43	54
10	DIGIN2	GPIOB12	42	55
11	DIGIN3	GPIOA11	25	85
12	DIGIN4	GPIOA12	24	86
13	DIGIN5	See Digital Input Source Selection 3.3.8.2		
14	DIGIN6			
15	DIGIN7			
16	DIGIN8			
17	DVCC			
18	GND			
19	DVCC			
20	GND			

Table 3-19: Digital I/O Mapping

3.3.8.1 Digital Interrupt Inputs

Six interrupt signals (XINT1A, XINT2, PDPINTA*, PDPINTB*, INDEXA and INDEXB) are available on a 16-pin IDC socket, **X10**, as shown in Figure 3-13. This provides the CPT-Mini2810 with externally triggered interrupts. The TTL level input signals are fully buffered (74LVX3245), with the buffer providing the level translation between the external 5V interface and the 3.3V core on the CPT-Mini2810. The mappings for the interrupts are given in Table 3-20.

Pin 1 of the digital interrupts connector, **X10**, is an off-card normally high reset signal. Any external connection to this signal should pull the signal momentarily LOW, to initiate a processor reset. Pull up resistors are located on the CPT-DA2810 board.

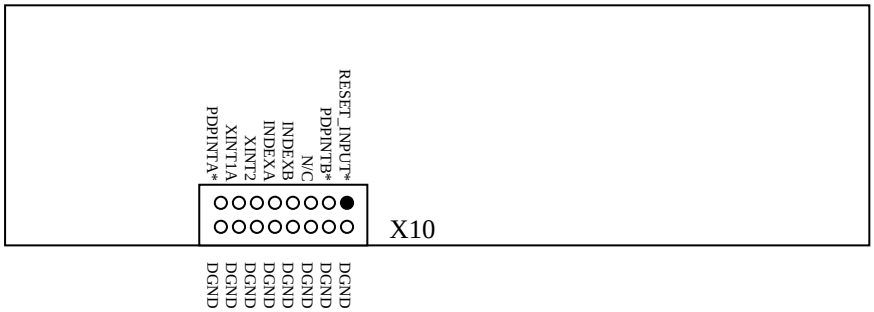


Figure 3-13: External Interrupt Connector (X10)

CONNECTOR X10, PIN	INTERRUPT SIGNAL	DSP MAPPING DEFINITION	CONNECTOR X8, PIN	CPT-DA2810 DSP PIN
15	PDPINTA*	PDPINTA*	23	81
13	XINT1A	See interrupt Source Selection	19	106
11	XINT2	XINT2	20	108
9	INDEXA	See Digital Input Source Selection		
7	INDEXB			
3	PDPINTB*	PDPINTB*	41	60

Table 3-20: Digital Interrupt Input Mapping

XINT1 can be sourced from either XINT1A, XINT1B. XINT1A is available on the **X10** interrupt connector and XINT1B is located on the MINI BUS connector, **X14**.

The response of the CPLD to XINT1A and XINT1B is configured by the INTSEL register (CPLD Address 0xC6), see Table 3-21 and Table 3-22. The active interrupt source is passed directly to the XINT1 interrupt to the CPT-DA2810. If both I1B and I1A are asserted, only XINT1A is enabled.

The data byte for the INTSEL register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	I1B	X	X	X	I1A

Table 3-21: INTSEL Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7 - 5	Reserved	
	4	I1B	Mini Bus interrupt source Mode (XINT1B) 0 Disabled 1 Enabled (only asserted if I1A = 0)
	3 – 1	Reserved	
	0	I1A	Interrupt header source Mode (XINT1A): 0 Disabled 1 Enabled (priority)

Table 3-22: SPI Bit allocation for INTSEL register

The default condition on power up is for both interrupt sources to be disabled.

3.3.8.2 Digital Input Source Selection

The 6 inputs DIGIN5 – DIGIN8 (on the Digital I/O connector) and INDEXA and INDEXB (on the Interrupt Input connector) can be configured for either standard digital inputs or peripheral mode. The available peripheral functions for these pins are the Capture Units or the Quadrature-Encoder Pulse (QEP) Circuits, as shown in Figure 3-14.

The TMS320F2810 DSP has QEP and CAP inputs for each Event Manager (EVA or EVB). To retain compatibility with existing Creative Power motherboards (CS-GIIB, CS-IIB, CS-IIC) the signals received on the CPT-Mini2810 board are able to be mapped to either Event Manager.

The six input signals (DIGIN5 – DIGIN8, INDEXA and INDEXB) are fed into the CPLD. The status of the CPLD CAPQEP register (Address 0xC4) selects the output location for the signals to either CAP1-3 or CAP4-6.

The DSP pins must be configured to capture port/QEP mode within the user code. Configuring these inputs within the CPLD only assigns the signal connection points on the CPT-DA2810 connector. It does not activate any DSP peripheral modes.

The data byte for the CAPQEP register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	CP

Table 3-23: CAPQEP Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7 – 1	Unused	
	0	CP	Capture Port Definition signal sourced from: 0 QEPB Mode: QEP allocated to EVB (ZX to EVA) 1 QEPA Mode: QEP allocated to EVA (ZX to EVB)

Table 3-24: SPI Bit allocation for CAPQEP register

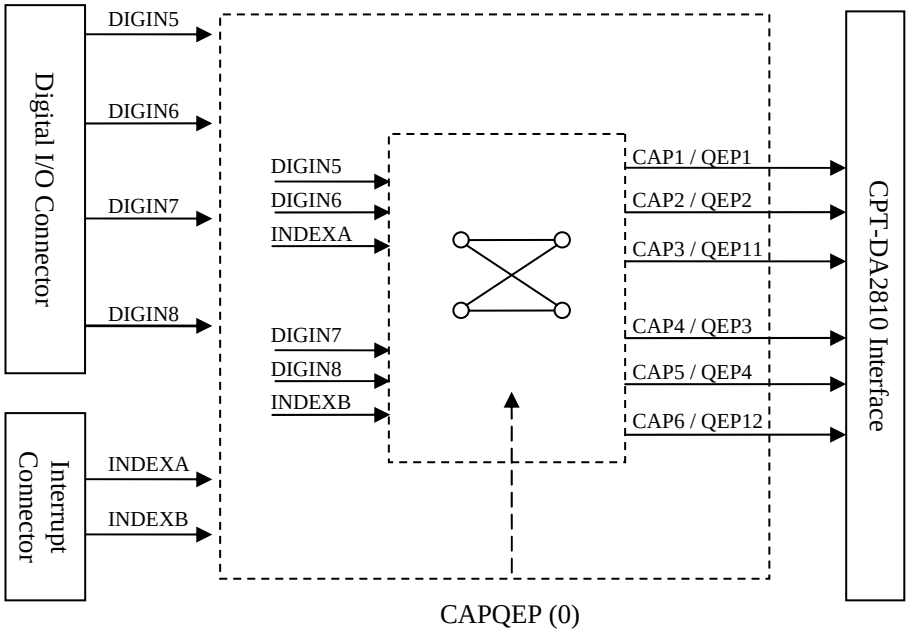


Figure 3-14: Capture Port Digital Input Configuration

Operation in QEPA mode (writing 0x01 to CAPQEP register) results in the following digital input mapping:

CPLD INPUT	CPLD OUTPUT	CONNECTOR X8, PIN	CPT-DA2810 DSP PIN
DIGIN5	CAP1	31	78
DIGIN6	CAP2	30	79
DIGIN7	CAP4	49	43
DIGIN8	CAP5	48	44
INDEX1	CAP3	29	80
INDEX2	CAP6	47	45

Table 3-25: QEPA Mode - 0x01 written to CAPQEP register

Operation in QEPB mode (writing 0x00 to CAPQEP register) results in the following digital input mapping:

CPLD INPUT	CPLD OUTPUT	CONNECTOR X8, PIN	CPT-DA2810 DSP PIN
DIGIN5	CAP4	49	43
DIGIN6	CAP5	48	44
DIGIN7	CAP1	31	78
DIGIN8	CAP2	30	79
INDEX1	CAP6	47	45
INDEX2	CAP3	29	80

Table 3-26: QEPB Mode - 0x00 written to CAPQEP register

On initial power up the CPLD defaults to QEPB mode.

3.3.9 PWM Interface

The CPT-Mini2810 can produce a maximum of 16 PWM outputs, with 8 PWM outputs (Event Manager A) available on PWM connector, **X3**. In addition, the 8 digital outputs on connector **X6** can be used as PWM outputs from Event Manager B (as specified in sections 3.1.5 and 3.3.8).

3.3.9.1 Even Manager A PWM Outputs

The CPT-Mini2810 has 8 PWM outputs from CPT-DA2810 EVA available on a 16-way IDC socket connector **X3**, see Figure 3-15. The CPT-Mini2810 outputs PWMA1 – PWMA8 are interleaved with digital ground (GND) to reduce noise between the channels. The signals are fully buffered (74LVX3245), which also provides level translation between the 3.3V core on the CPT-Mini2810 and the 5V output for use by an external gate driver card or an electrical to optical conversion-card (SP1-FOP1).

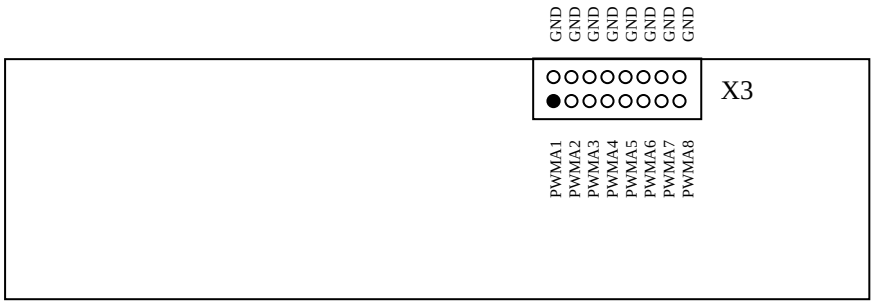


Figure 3-15: Gate Driver Interface (PWM) Connector

The EVA gate fault signal (PDPINTA*) is available on connector **X10** for fast disabling of the Event Manager A PWM outputs.

CPT-DA2810 Event Manager A can produce up to 8 PWM waveforms: 3 independent pairs (6 outputs) from the three full-compare units, with DSP programmable deadbands, and two independent PWMs from the GP-timer compares.

The 2 GP-timer compare outputs from Event Manager A can be configured with the EVACOMCON register as either pass-through connections, or T1PWM can be configured to generate complementary PWM outputs on PWMA7 and PWMA8. The deadband for the complementary outputs can be set in the EVACONDB register.

If individual gate fault signal status is required they can be read back via the Mini Bus interface.

The PWMAx outputs from the CPLD must be enabled before they can be used. The mode of operation for each PWMAx output is selected within the EVACOMCON register (Address 0xD0) as defined in Table 3-27, Table 3-28, Table 3-29 and Table 3-30. To enable PWMA1 to PWMA8 bit 0 (ENA) is asserted. In the event of a PDPINTA* fault the ENA bit is reset to 0 and the PWMA1-PWMA8 outputs are disabled. ENA cannot be asserted unless the PDPINTA* input is high, to provide power stage protection.

Please note that the internal computation PWM functionality is not included with the standard CPT-Mini2810.

The data byte for the EVACOMCON register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
T1M	P6	P5	P4	P3	P2	P1	ENA

Table 3-27: EVACOMCON Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	T1M	Output Mode Selection for PWMA7 and PWMA8 0 PWM7A/ PWM8A as Digital Outputs (pass through) 1 T1PWM as Complementary PWM on PWMA7 and PWMA8
	6	P6	Output Mode Selection for PWMA6 0 Sourced from PWM6 Input (pass through) 1 Internal Computation
	5	P5	Output Mode Selection for PWMA5 0 Sourced from PWM5 Input (pass through) 1 Internal Computation
	4	P4	Output Mode Selection for PWMA4 0 Sourced from PWM4 Input (pass through) 1 Internal Computation
	3	P3	Output Mode Selection for PWMA3 0 Sourced from PWM3 Input (pass through) 1 Internal Computation
	2	P2	Output Mode Selection for PWMA2 0 Sourced from PWM2 Input (pass through) 1 Internal Computation
	1	P1	Output Mode Selection for PWMA1 0 Sourced from PWM1 Input (pass through) 1 Internal Computation
	0	ENA	PWM Output Enable 0 Disable – outputs P1-P6 and PWMA7 & PWMA8 are set to 0 1 Enable – outputs are set depending on status of P1-P6,T1M

Table 3-28: EVACOMCON Register Bit Definitions

When configured as simple compare outputs (T1M bit = 1), T1PWM can be used to generate complementary outputs PWMA7 / PWMA8 with a CPLD programmable deadband defined within the EVACONDB register (Address 0xD2). This register has the same structure for scaling as the TMS320F281x internal deadband generator.

The data byte for the EVACONDB register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
EDBT	DBT3	DBT2	DBT1	DBT0	DBTPS2	DBTPS1	DBTPS0

Table 3-29: EVACONDB Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	EDBT	Enable Deadband Generator for T1M = 1, ignored if T1M = 0 0 Disabled 1 Enabled
	6 – 3	DBT3 – DBT0	Dead-band timer period. These bits define the period value of the 4-bit dead band timers
	2 – 0	DBTPS2 – DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 x = Device (CPU) clock frequency

Table 3-30: EVACONDB Register Bit Definitions

3.3.9.2 Event Manager B PWM Outputs

The CPT-Mini2810 digital output bank can be configured to generate 8 PWM signals which are sourced from Event Manager B on the CPT-DA2810 interface.

The connector contains:

- 8 PWM output signals (PWMB1 – PWMB8 along with 8 digital inputs, DVCC and GND)

A gate fault signal (PDPINTB*) is available on connector **X10** for fast disabling of the Event Manager B PWM outputs.

If individual gate fault signal status is required they can be read back via the Mini Bus interface.

The mode of operation for PWMB7 and PWMB8 output is selected within the EVBCOMCON register (Address 0xD4).

The 2 GP-timer compare outputs from Event Manager B can be configured with the EVBCOMCON register as either pass-through connections, or T3PWM can be configured to generate complementary PWM outputs on PWMB7 and PWMB8. The deadband for the complementary outputs can be set in the EVBCONDB register.

To enable outputs PWMB7 and PWMB8 in complementary mode, bit 0 (ENB) is asserted. In the event of a PDPINTB* fault the ENB bit is reset to 0 and the PWMB7 and PWMB8 outputs are disabled. ENB cannot be asserted unless the PDPINTB* input is high, to provide power stage protection. Note: PDPINTB* does not disable the pass-through connection for PWMB7 and PWMB8 (this is managed directly by the TMS320F2810).

The data byte for the EVBCOMCON register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
T3M	X	X	X	X	X	X	ENB

Table 3-31: EVBCOMCON Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	T3M	Output Mode Selection for PWMB7 and PWMB8 0 PWMB7/ PWMB8 as Digital Outputs (pass through) 1 T3PWM as Complementary PWM on PWMB7 and PWMB8
	6 – 1	Reserved	
	0	ENB	PWMB7/B8 Output Enable 0 Disable – PWMB7 & PWMB8 set to 0 if T3M = 1 1 Enable – PWMB7 & PWMB8 set on status of T3M

Table 3-32: EVBCOMCON Register Bit Definitions

When configured as simple compare outputs (T3M bit = 1), T3PWM can be used to generate complementary outputs PWMB7 / PWMB8 with a CPLD programmable deadband defined within the EVBCONDB register (Address 0xD6). This register has the same structure for scaling as the TMS320F281x internal deadband generator.

The data byte for the EVBCONDB register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
EDBT	DBT3	DBT2	DBT1	DBT0	DBTPS2	DBTPS1	DBTPS0

Table 3-33: EVACONDB Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	EDBT	Enable Deadband Generator for T3M = 1, ignored if T3M = 0 0 Disabled 1 Enabled
	6 – 3	DBT3 – DBT0	Dead-band timer period. These bits define the period value of the 4-bit dead band timers
	2 – 0	DBTPS2 – DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 x = Device (CPU) clock frequency

Table 3-34: EVBCONDB Register Bit Definitions

3.3.10 Analog Switch Selection

There are 11 analog switches on the CPT-Mini2810 board. 4 of these are controlled directly from the CPT-DA2810 GPIO pins (as described in 3.3.6) and the remaining 7 can be set through the SPI Interface via the ANLGSW register.

The seven analog switches for the hysteresis controller are separated into 4 source switches (INA – IND) and 3 configuration switches (IN1 – IN3). The status of the CPLD ANLGSW register (Address 0xD8) selects the status of each of these analog switches.

The data byte for the ANLGSW register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
HE	IN3	IN2	IN1	IND	INC	INB	INA

Table 3-35: ANLGSW Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	HE	Hysteresis Enable 0 PWM Signals sourced from EVA inputs 1 PWM Signals sourced from Hysteresis input
	6	IN3	Hysteresis band error signal sourced from: 0 DAC4/MEAS4 1 (IN2=1) DAC1/MEAS1 (IN2=0) DAC3/MEAS3
	5	IN2	Hysteresis band error signal sourced from: 0 DAC3/MEAS3 1 DAC1/MEAS1
	4	IN1	Hysteresis band error signal sourced from: 0 DAC2/MEAS2 1 DAC1/MEAS1
	3	IND	Hysteresis input MEAS3 selected from analog: 0 ADC5 1 ADC8
	2	INC	Hysteresis input MEAS4 selected from analog: 0 ADC4 1 ADC12
	1	INB	Hysteresis input MEAS2 selected from analog: 0 ADC10 1 ADC11
	0	INA	Hysteresis input MEAS1 selected from analog: 0 ADC2 1 ADC3

Table 3-36: Analog Switch Bit allocation for ANLGSW register

3.3.11 GPIO and Test Point Digital I/O Selection

There are 3 digital input/output signals in the CPLD that can be used to test the functionality of the CPLD program and the operation of the CPT-Mini2810 board. The direction of these signals can be set via the GPIO register (Address 0xDA) bits 6-4, and the value set/read on bits 2-0. By default the three bits are set up to be outputs from the CPLD.

The data byte for the GPIO register, BYTE 1, has the following format:

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	T1D	F7D	D1D	X	T1	F7	D1

Table 3-37: GPIO Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	Reserved	
	6	T1D	Direction of CPLD Pin TP3 (pin 53) 0 = Input (Default), 1 = Output
	5	F7D	Direction of CPLD Pin GPIOF7 (pin 54) 0 = Input, 1 = Output (Default)
	4	D1D	Direction of CPLD Pin GPIOD1 (pin 55) 0 = Input, 1 = Output (Default)
	3	Reserved	
	2	T1	CPLD Pin TP3 (pin 53): Set to 0/1 if T1D=1
	1	F7	CPLD Pin GPIOF7 (pin 54): Set to '0' if F7D=1
	0	D1	CPLD Pin GPIOD1 (pin 55): Set to '0' if D1D=1

Table 3-38: Bit allocation for GPIO register

3.3.12 DATELO, DATEHI and VERSION Registers

There are 3 registers used in the CPLD to store the compile date and version of the CPLD software that has been loaded. DATEHI and DATELO are 8 bit registers that between them store the day, month and year of the compiled CPLD code. Day is 5 bits, representing 1-31, Month is 4 bits representing 1-12 and Year is 7 bits representing 2000 to 2127. The VERSION register stores the current version of the CPLD software to one decimal place. (For example a value of 21 is version 2.1). These registers have the following format.

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Y	Y	Y	Y	Y	Y	Y	M

Table 3-39: DATEHI Register Data Byte Structure

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
M	M	M	D	D	D	D	D

Table 3-40: DATELO Register Data Byte Structure

BYTE	BIT(S)	NAME	DESCRIPTION
DATEHI	15 – 9	Y	Year – in binary format (0-127) (2000-2127)
	8	M	Month – in binary format (1-12)
DATELO	7 – 5	M	
	4 – 0	D	Day of the Month – in binary format (1 – 31)

Table 3-41: Bit allocation for DATEHI and DATELO registers

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
V	V	V	V	V	V	V	V

Table 3-42: VERSION Register Data Byte Structure

Note: For CPLD versions prior to V2.1 a read to any of these three registers will return the value 0x00.

3.3.13 SPECIAL function Register

The special function register is used for USER programmed CPLD functionality. If a user has added their own code (such as hysteresis operation) into the base CPLD code, this code is enabled/accessed via the special function register. The user modifies the CPLD code structures at their own risk.

The SPECIAL register is not used with the default supplied CPLD code.

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Table 3-43: SPECIAL Register Data Byte Structure

3.4 Power Supply Interface

The power supplies for the CPT-Mini2810 are supplied via the IDC sockets on the underside of the board. The board requires analog ±15V as well as +5V digital. The ±15V/AGND must be supplied via the **X2** connector and the +5V/GND digital must be supplied via connectors **X6, X9** and **X14**, as shown in Figure 3-16.

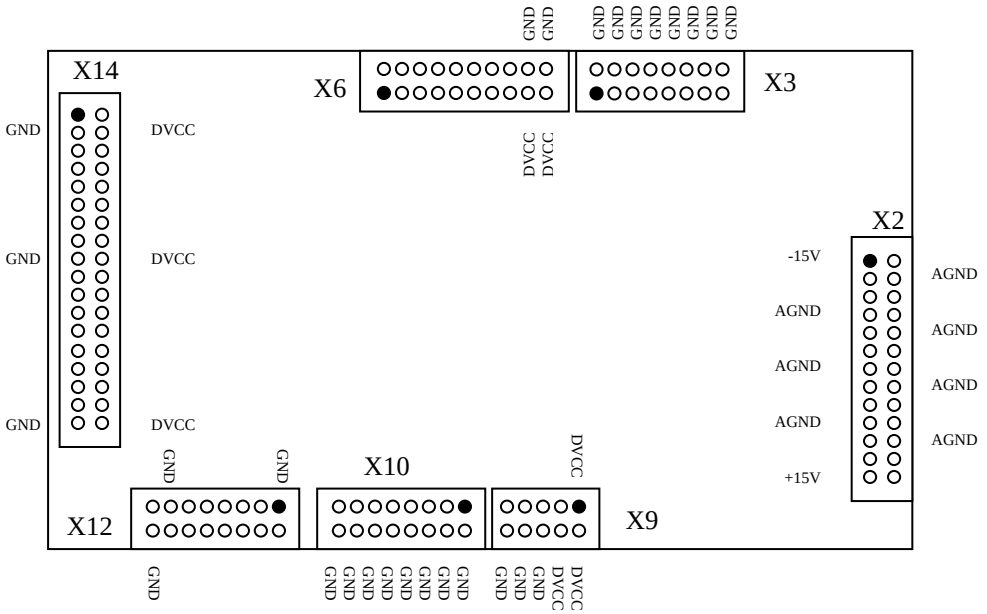
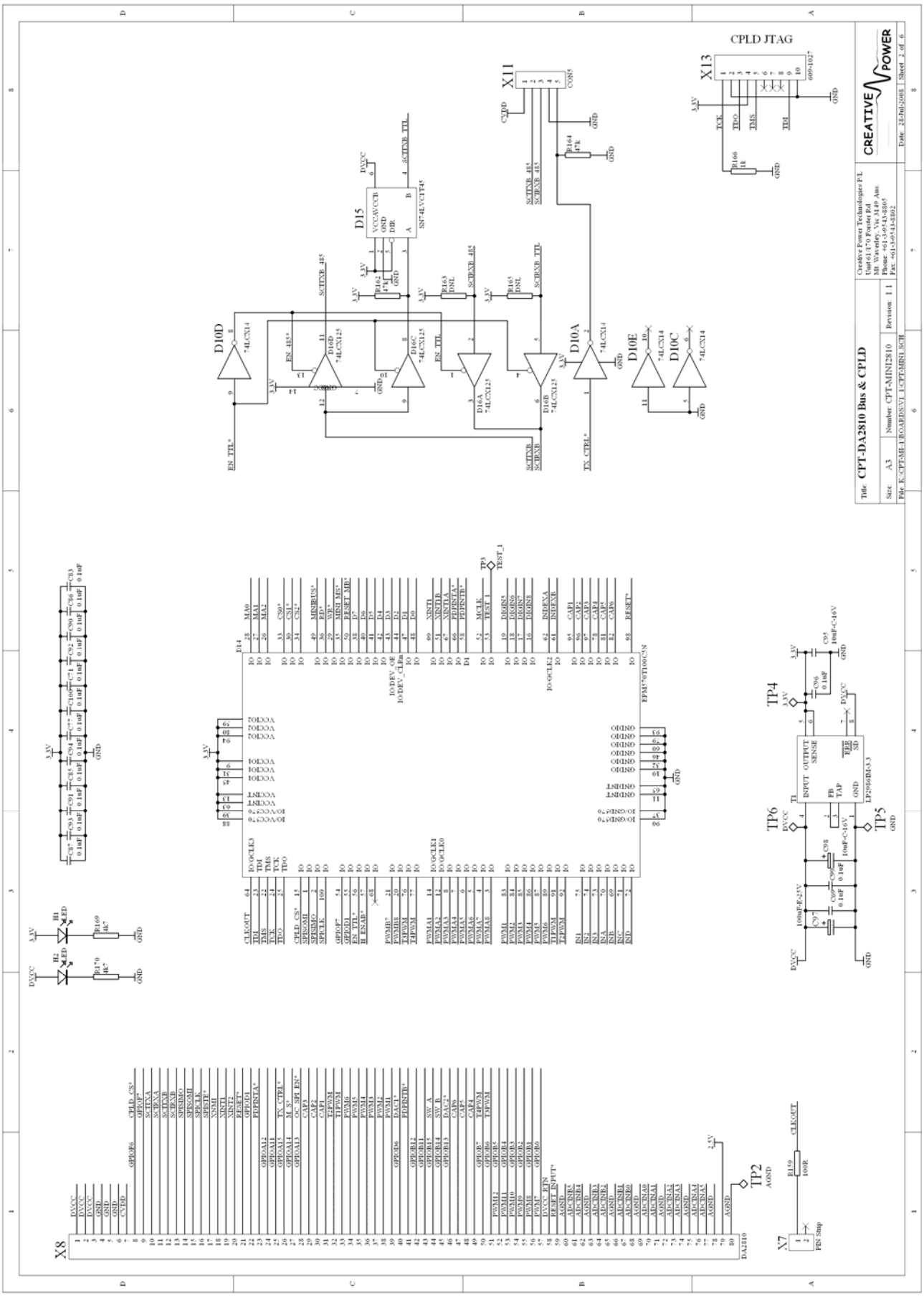
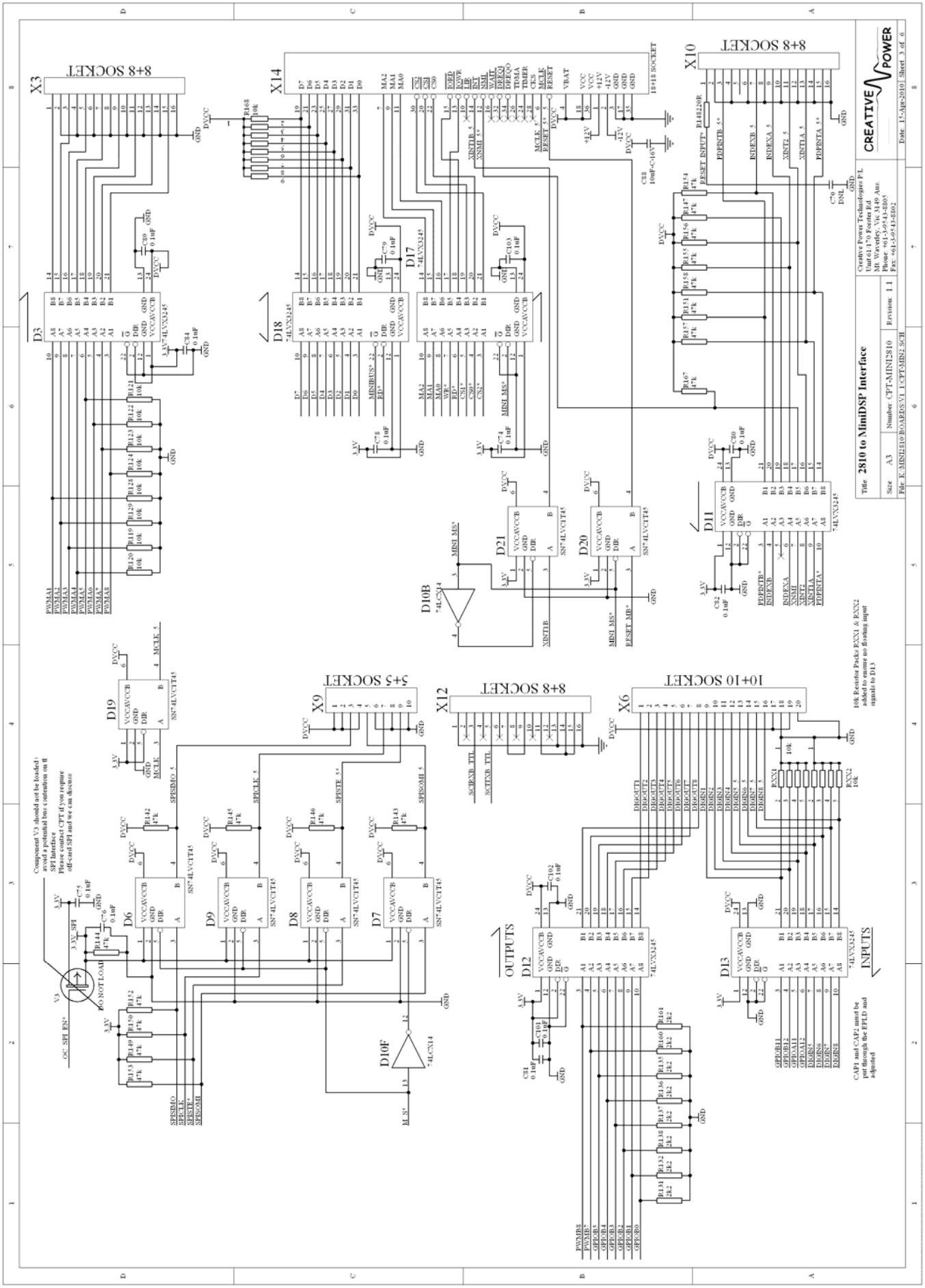


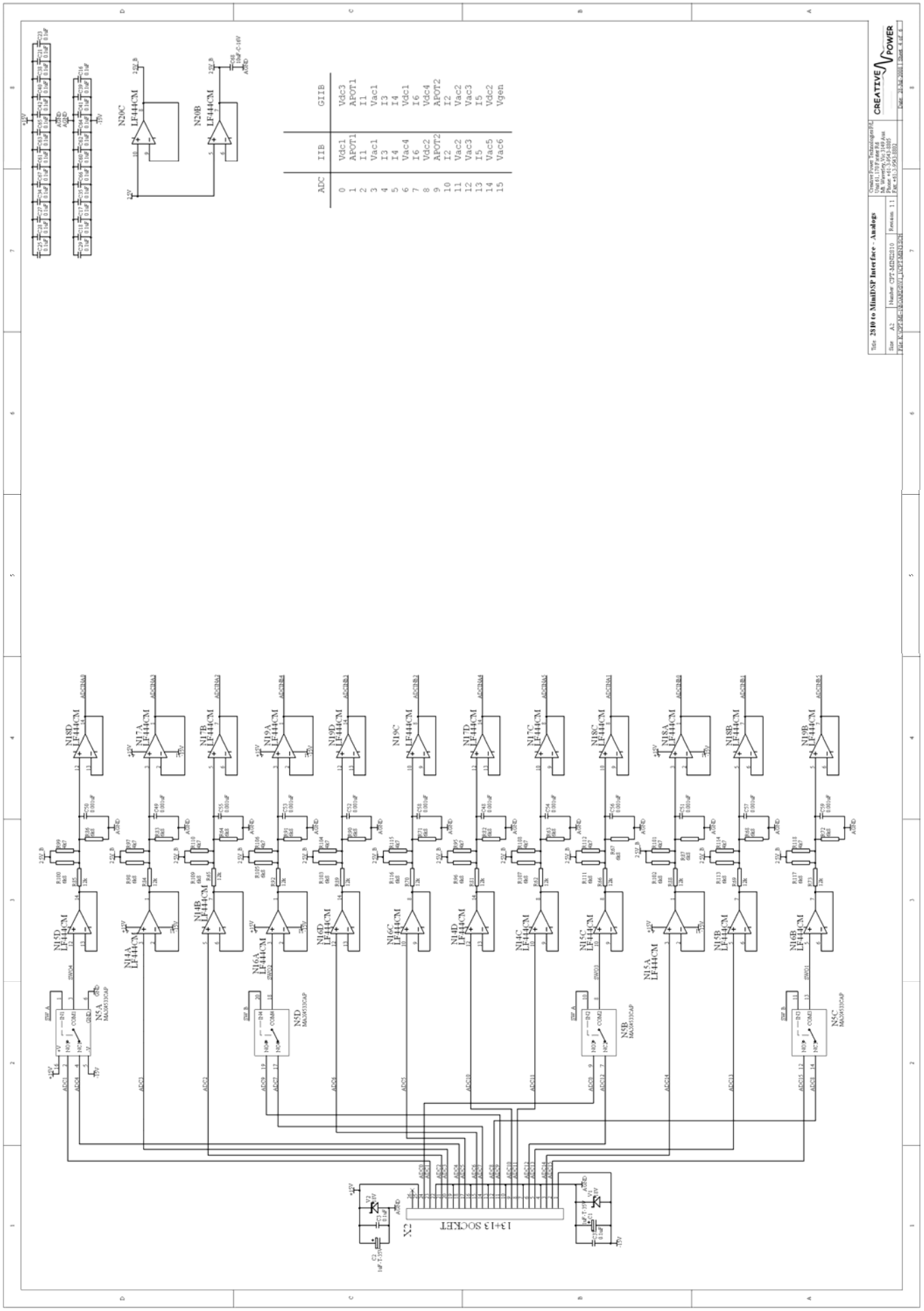
Figure 3-16: Plug-in Power Supply Connector Configuration

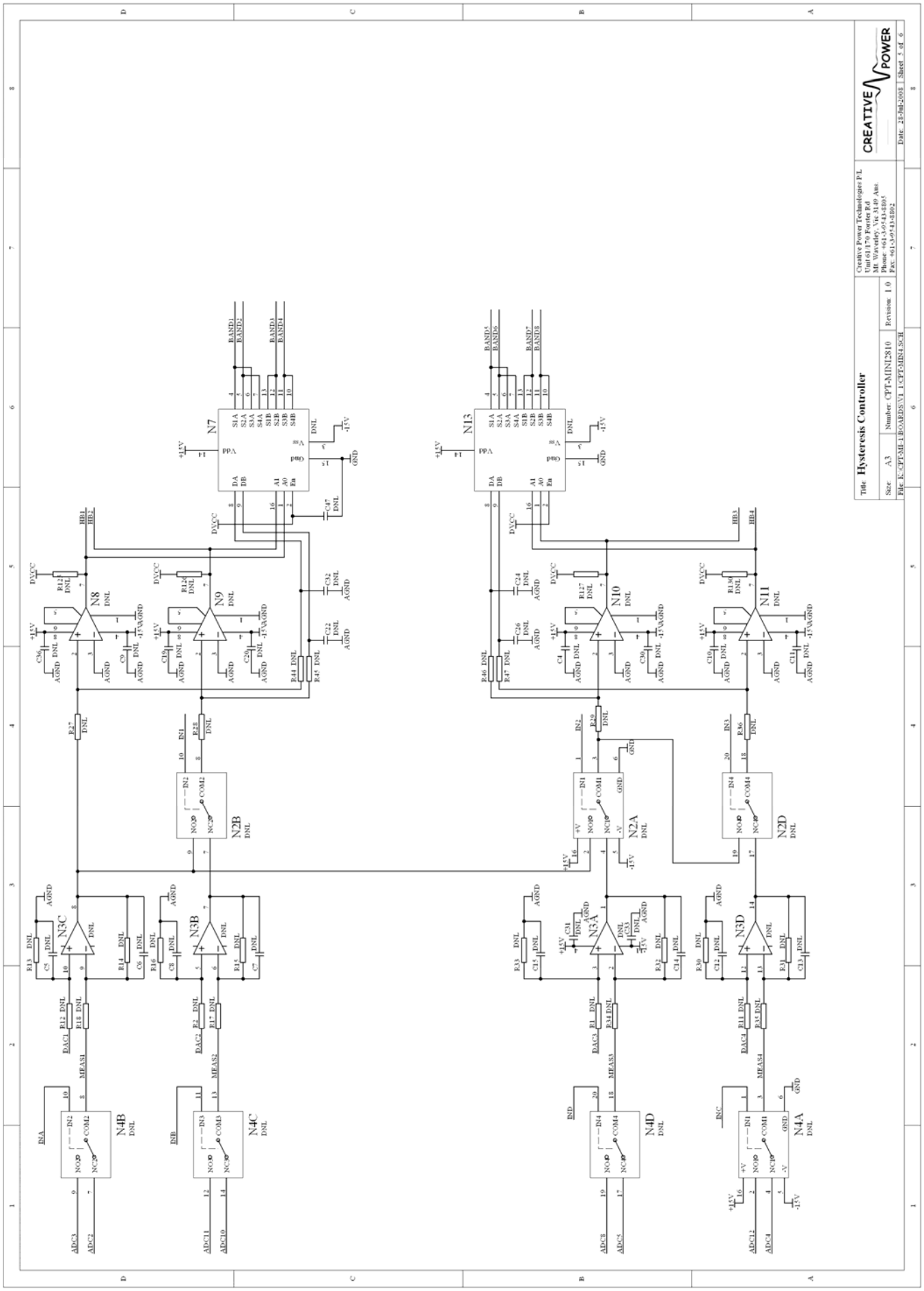
Appendix

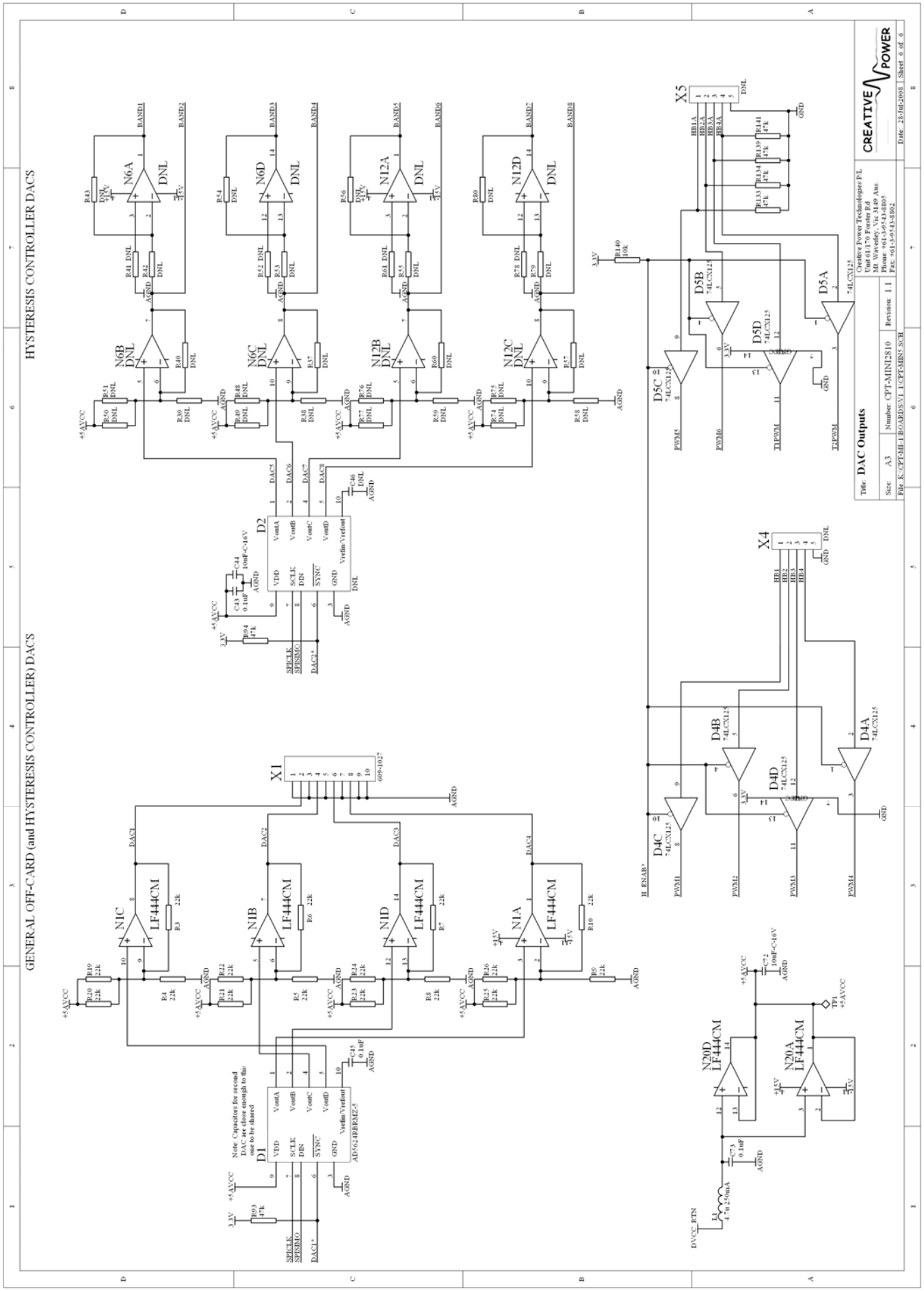
Appendix A Schematic Diagrams




Title 2810 to MiniDSP Interface
Creative Power Technologies P/L
Unit 6 1 17 0 Foster Rd
Mt Waverley, Vic 3149 Aus
Phone: +61-3-9543-8805
Fax: +61-3-9543-8802
Size A3
Number CPT-MINI2810
Revision 1.1
Date: 15-Apr-2010 Sheet 3 of 6
File: K:\MINI2810\BOARDS\V1 1\CPT-MIN2 SCH
CREATIVE POWER
X3 8+8 SOCKET
X14 18*18 SOCKET
X10 8+8 SOCKET
X12 8+8 SOCKET
X9 5+5 SOCKET
X6 10+10 SOCKET
D3 D18 D17 D21 D20 D11 D19 D6 D9 D8 D7 D10B D10F D12 D13
OUTPUTS
INPUTS
Component V3 should not be loaded to avoid a potential bus contention on the SPI Interface
Please contact CPT if you require old-card SPI and we can discuss
DO NOT LOAD
10k Resistor Packs RXX1 & RXX2 added to ensure no floating input signals to D13
CAP1 and CAP2 must be put through the EFLD and adjusted

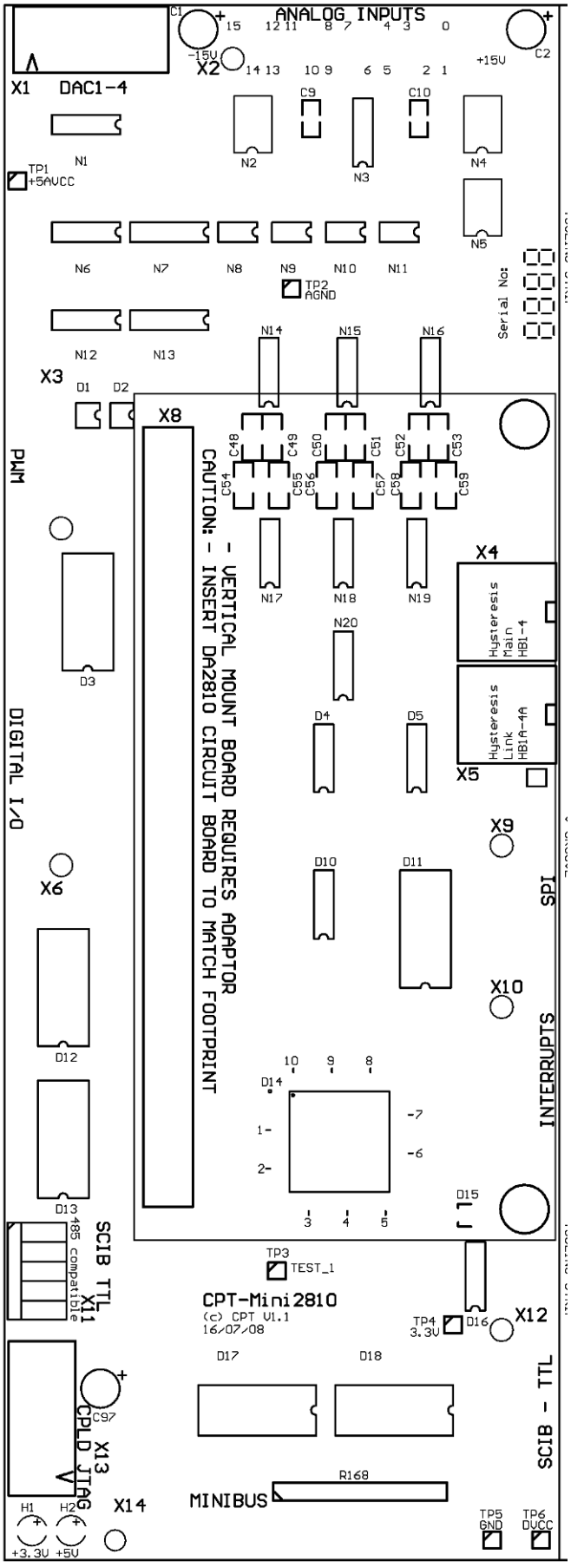

ADC IIB GIIB
0 Vdc1 Vdc3
1 APOT1 APOT1
2 I1 I1
3 Vac1 Vac1
4 I3 I3
5 I4 I4
6 Vac4 Vdc1
7 I6 I6
8 Vdc2 Vdc4
9 APOT2 APOT2
10 I2 I2
11 Vac2 Vac2
12 Vac3 Vac3
13 I5 I5
14 Vac5 Vdc2
15 Vac6 Vgen
13+13 SOCKET
CREATIVE POWER


Title: Hysteresis Controller
Size: A3
Number: CPT-MINI2810
Revision: 1.0
Date: 28-Jul-2008
Sheet 5 of 6
File: K:\CPT-ME-1\BOARDS\V1.1\CPT-MB14.SCH
Creative Power Technologies P/L
Unit 61/170 Forster Rd
Mt Waverley, Vic 3149 Aus.
Phone: +61-3-9543-4555
Fax: +61-3-9543-8892
CREATIVE POWER
N7
N8
N9
N10
N11
N13
N2A
N2B
N2C
N2D
N3A
N3B
N3C
N3D
N4A
N4B
N4C
N4D

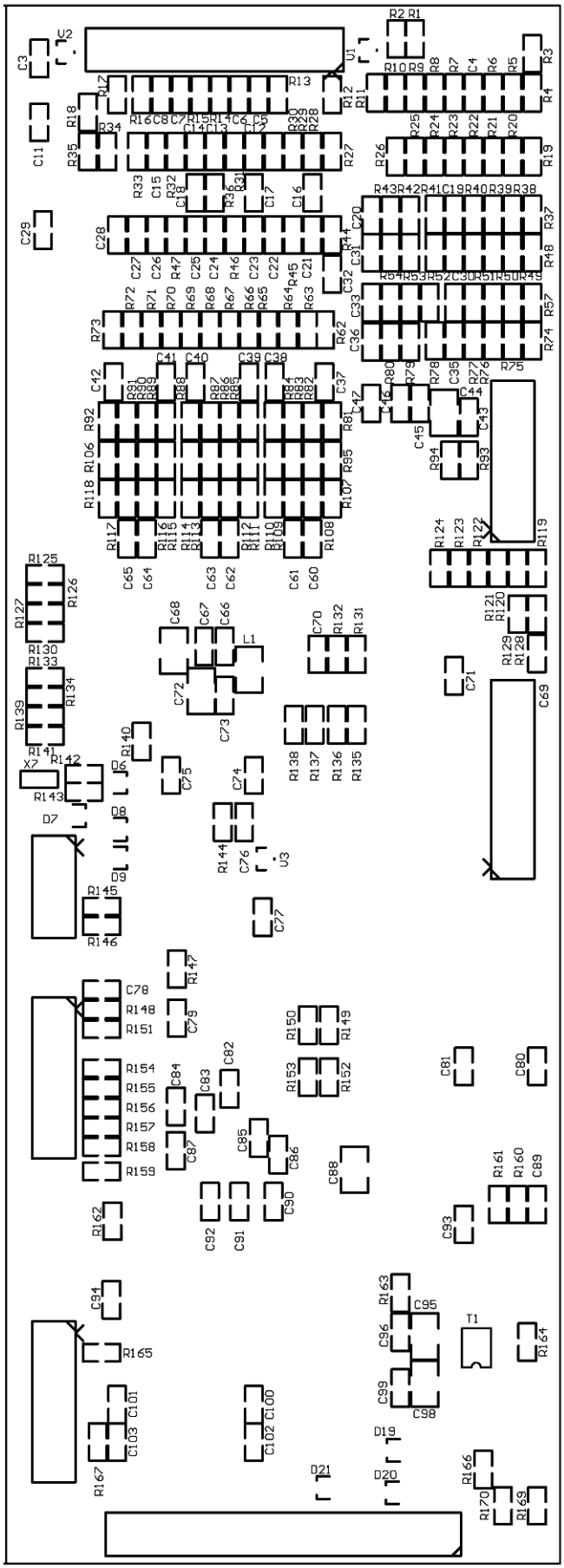

HYSTERESIS CONTROLLER DACS
GENERAL OFF-CARD (and HYSTERESIS CONTROLLER) DACS
Title: DAC Outputs
Size: A3
Number: CPT-MINI2810
Revision: 1.1
File: K:\CPT-MB-I BOARDS\V1 1\CPT-MINI5.SCH
Creative Power Technologies P/L
Unit 61/170 Foster Rd
Mt Waverley, Vic 3149 Aus
Phone: +61-3-9543-8305
Fax: +61-3-9543-9802
Date: 28-Jul-2008
Sheet 6 of 6
CREATIVE POWER
Note: Capacitors for record DAC are close enough to fan one to be shared
AD5624RBRMZ-5
LF444CM
74LCX125

Appendix B Component Layout

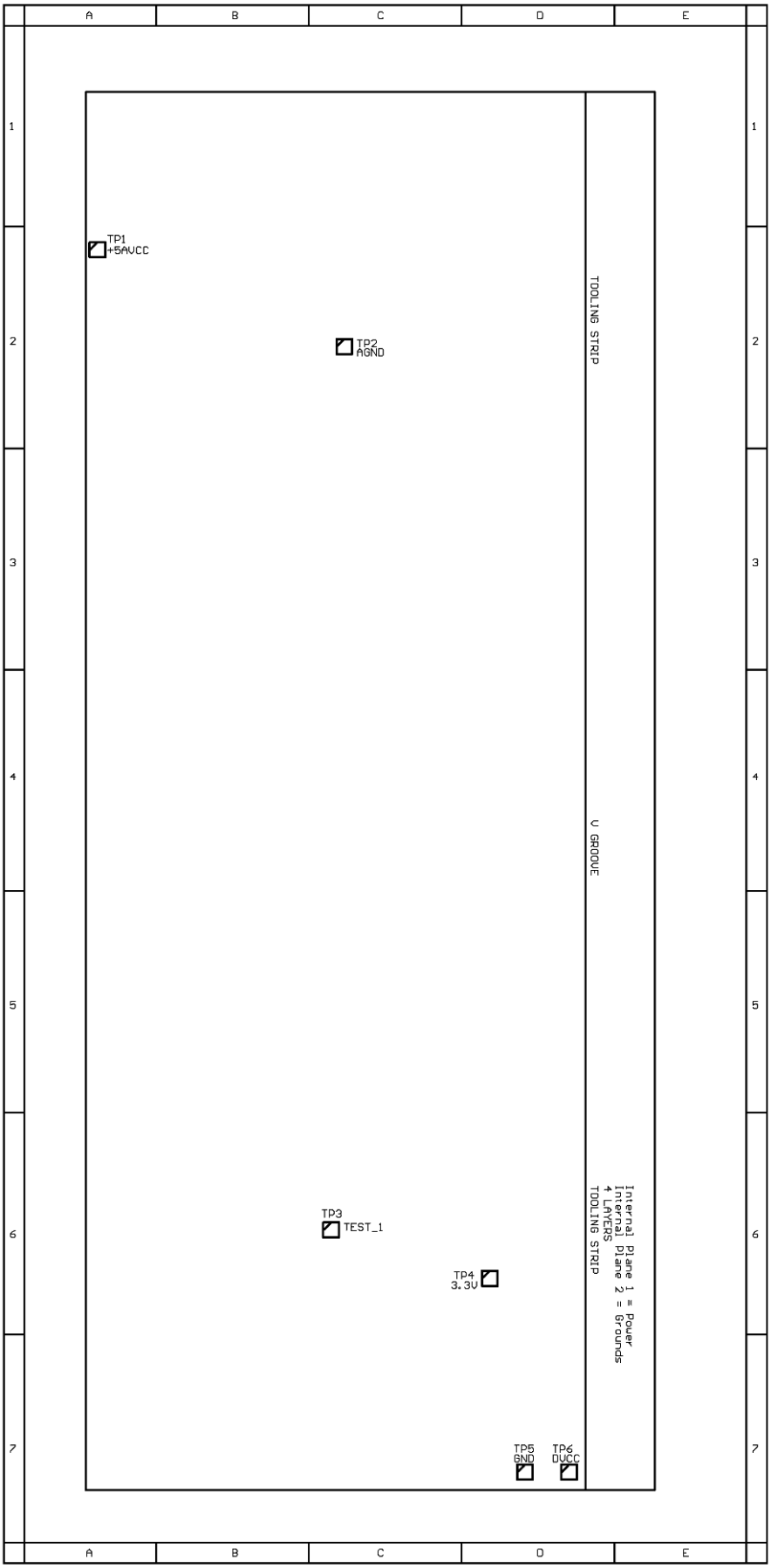
Top Layer



Bottom Layer



Appendix C Test Point Locations



Appendix D Connector Pinouts

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Analog Inputs				
X2	CON26 609-2627 (26-way IDC Socket)	1	-15V	Negative Regulated Analog Supply Input
		2	ADC15	Analog Input 15
		3	ADC14	Analog Input 14
		4	AGND	Analog Ground
		5	ADC13	Analog Input 13
		6	ADC12	Analog Input 12
		7	AGND	Analog Ground
		8	ADC11	Analog Input 11
		9	ADC10	Analog Input 10
		10	AGND	Analog Ground
		11	ADC9	Analog Input 9
		12	ADC8	Analog Input 8
		13	AGND	Analog Ground
		14	ADC7	Analog Input 7
		15	ADC6	Analog Input 6
		16	AGND	Analog Ground
		17	ADC5	Analog Input 5
		18	ADC4	Analog Input 4
		19	AGND	Analog Ground
		20	ADC3	Analog Input 3
		21	ADC2	Analog Input 2
		22	AGND	Analog Ground
		23	ADC1	Analog Input 1
		24	ADC0	Analog Input 0
		25	+15V	Positive Regulated Analog Supply Input
		26	N/C	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Interrupt Input Port				
X10	CON16 609-1627 (16-way IDC Socket)	1	RESET_INPUT*	External Reset Input
		2	GND	
		3	PDPINTB*	Interrupt Input
		4	GND	
		5	N/C	
		6	GND	
		7	INDEXB	Interrupt Input – to Capture Port 6/3
		8	GND	
		9	INDEXA	Interrupt Input – to Capture Port 3/6
		10	GND	
		11	XINT2	Interrupt Input – to XINT2
		12	GND	
		13	XINT1A	Interrupt Input – to CPLD
		14	GND	
		15	PDPINTA*	Interrupt Input
		16	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Gate Driver Interface Connectors				
X3	CON16 609-1627 (16-way IDC Socket)	1	PWMA1	Upper ***A*** Phase Gate Signal – Logic
		2	GND	
		3	PWMA2	Lower ***A*** Phase Gate Signal – Logic
		4	GND	
		5	PWMA3	Upper ***B*** Phase Gate Signal – Logic
		6	GND	
		7	PWMA4	Lower ***B*** Phase Gate Signal – Logic
		8	GND	
		9	PWMA5	Upper ***C*** Phase Gate Signal – Logic
		10	GND	
		11	PWMA6	Lower ***C*** Phase Gate Signal – Logic
		12	GND	
		13	PWMA7	Upper ***D*** Phase Gate Signal – Logic
		14	GND	
		15	PWMA8	Lower ***D*** Phase Gate Signal – Logic
		16	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Digital I/O Port				
X6	CON20 609-2027 (20-way IDC socket)	1	DIGOUT0/PWMB1	Logic Level Digital Output
		2	DIGOUT1/PWMB2	Logic Level Digital Output
		3	DIGOUT2/PWMB3	Logic Level Digital Output
		4	DIGOUT3/PWMB4	Logic Level Digital Output
		5	DIGOUT4/PWMB5	Logic Level Digital Output
		6	DIGOUT5/PWMB6	Logic Level Digital Output
		7	DIGOUT6/PWMB7	Logic Level Digital Output
		8	DIGOUT7/PWMB8	Logic Level Digital Output
		9	DIGIN1/GPIOB11	Logic Level Digital Input
		10	DIGIN2/GPIOB12	Logic Level Digital Input
		11	DIGIN3/GPIOA11	Logic Level Digital Input
		12	DIGIN4/GPIOA12	Logic Level Digital Input
		13	DIGIN5	Logic Level Digital Input
		14	DIGIN6	Logic Level Digital Input
		15	DIGIN7	Logic Level Digital Input
		16	DIGIN8	Logic Level Digital Input
		17	DVCC	
		18	GND	
		19	DVCC	
		20	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Communications – SCIB– TTL Level				
X12	CON16 609-1627 (16-way IDC Socket)	1	GND	
		2	N/C	
		3	SCIRXB_TTL	LVTTL Level Receive Signal
		4	N/C	
		5	SCITXB_TTL	LVTTL Level Transmit Signal
		6	N/C	
		7	To pin 9	
		8	N/C	
		9	To pin 7	
		10	N/C	
		11	To pin 14, 15	
		12	N/C	
		13	GND	
		14	To pin 11,15	
		15	To pin 11,14	
		16	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Communications – SCIB – TTL Level (with Transmit Control)				
X11	MASCON5 (Molex 5-way Header)	1	CVDD	
		2	SCITXB_485	LVTTL Level Transmit Signal
		3	SCIRXB_485	LVTTL Level Receive Signal
		4	GND	
		5	TX_CTRL	Transmit Control (RS-422/485 mode)
Communications – Clocked Serial Port				
X9	CON10 609-1027 (Shrouded 10-way IDC Header)	1	DVCC	
		2	DVCC	
		3	SPISIMO	SPI Data Output (Master)
		4	DVCC	
		5	SPISOMI	SPI Data Input (Master)
		6	GND	
		7	SPICLK	SPI Clock Signal
		8	GND	
		9	SPISTE*	SPI Transmit/Chip Enable
		10	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
CPLD JTAG				
X13	CON10 609-1027 (Shrouded 10-way IDC Header)	1	TCK	JTAG Clock Signal
		2	GND	
		3	TDO	JTAG Output Signal
		4	3.3V	
		5	TMS	JTAG Enable
		6	N/C	
		7	N/C	
		8	N/C	
		9	TDI	JTAG Input Signal
		10	GND	

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Mini Bus Interface – All Versions				
X14	Mini Bus DIL36 (36-way socket)	1	N/C	Nominal +12V connection – not available on CPT-Mini2810 V1.1 PCB
		2	N/C	Nominal -12V connection – not available on CPT-Mini2810 V1.1 PCB
		3	GND	Digital Ground
		4	DVCC	+5V Logic Supply
		5	RESET_MB*	Mini Bus Reset – CPLD can trigger
		6	MCLK	MCLK from DSP's CLKOUT
		7	MA2	Buffered Address Line 2 (MA_2)
		8	N/C	
		9	MA1	Buffered Address Line 1 (MA_1)
		10	N/C	
		11	MA0	Buffered Address Line 0 (MA_0)
		12	XNMI*	Buffered Non-Maskable Interrupt
		13	WR*	Buffered Write Signal (WR*)
		14	XINT1B	Buffered Interrupt
		15	RD*	Buffered Read Signal
		16	N/C	
		17	GND	Digital Ground
		18	DVCC	+5V Logic Supply
		19	D7	Buffered Address/Data Line
		20	CS1*	Buffered Chip Select Line 1
		21	D6	Buffered Address/Data Line
		22	CS0*	Buffered Chip Select Line 0
		23	D5	Buffered Address/Data Line
		24	N/C	
		25	D4	Buffered Address/Data Line
		26	N/C	
		27	D3	Buffered Address/Data Line
		28	N/C	
		29	D2	Buffered Address/Data Line
		30	CS2*	Buffered Chip Select Line 2
		31	D1	Buffered Address/Data Line
		32	N/C	
		33	D0	Buffered Address/Data Line
		34	N/C	
		35	GND	Digital Ground
		36	DVCC	+5V Logic Supply

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Main DSP Connector				
X8	80-way IDC Socket (Top Side)	1	DVCC	+5V Input Supply
		2	DVCC	+5V Input Supply
		3	DVCC	+5V Input Supply
		4	GND	Digital Ground
		5	GND	Digital Ground
		6	GND	Digital Ground
		7	CVDD	3.3V supply
		8	GPIOF6	CPLD_CS* - Chip Select for CPLD
		9	GPIOF7	GPIOF7 to CPLD
		10	SCITXA	Not Used on CPT-Mini2810
		11	SCIRXA	Not Used on CPT-Mini2810
		12	SCITXB	SCI asynchronous serial port B TX
		13	SCIRXB	SCI asynchronous serial port B RX
		14	SPISIMO	SPI slave input, master output
		15	SPISOMI	SPI slave out, master input
		16	SPICLK	SPI clock
		17	SPISTE*	SPI slave transmit enable
		18	XNMI	XINT13 or Non-maskable Interrupt
		19	GPIOE0 / XINT1	GPIO or External Interrupt 1
		20	XINT2	External Interrupt 2
		21	RESET*	Reset Output
		22	GPIOD1	GPIOD1 to CPLD
		23	PDPINTA*	Gate Fault Trip Signal EVA
		24	GPIOA12	Digital Input 4
		25	GPIOA11	Digital Input 3
		26	GPIOA15	TX_CTRL – Transmit Control
		27	GPIOA14	M_S* – Master/Slave SPI selection
		28	GPIOA13	OC_SPI_EN – off-card SPI enable
		29	GPIOA10 / CAP3	INDEXA / INDEXB / CAP3 / QEPI1
		30	GPIOA9 / CAP2	DIGIN6 / DIGIN8 / CAP2 / QEP2
		31	GPIOA8 / CAP1	DIGIN5 / DIGIN7 / CAP1 / QEP1
		32	GPIOA7 / T2PWM	GPIO / Timer 2 Output Trip
		33	GPIOA6 / T1PWM	GPIO / Timer 1 Output Trip
		34	GPIOA5 / PWM6	GPIO / PWM output pin 6
		35	GPIOA4 / PWM5	GPIO / PWM output pin 5
		36	GPIOA3 / PWM4	GPIO / PWM output pin 4
		37	GPIOA2 / PWM3	GPIO / PWM output pin 3
		38	GPIOA1 / PWM2	GPIO / PWM output pin 2
		39	GPIOA0 / PWM1	GPIO / PWM output pin 1
		40	GPIOD6	DAC1* - Chip Select
		41	GPIOD5 / PDPINTB*	GPIO or Gate Fault B*
		42	GPIOB12	Digital Input 2
		43	GPIOB11	Digital Input 1
		44	GPIOB15	SW_A – Analog Chanel A Switch Selection
		45	GPIOB14	SW_B – Analog Chanel B Switch Selection
		46	GPIOB13	DAC2* - Chip Select
		47	GPIOB10 / CAP6	INDEXB / INDEXA / CAP6 / QEPI2
		48	GPIOB9 / CAP5	DIGIN8 / DIGIN6 / CAP5 / QEP4
		49	GPIOB8 / CAP4	DIGIN7 / DIGIN5 / CAP4 / QEP3
		50	GPIOB7 / T4PWM	GPIO / Timer 4 Output Trip

Conn. No.	Connector Type	Pin No.	Signal Name	Comments
Main Connector (continued)				
X8 Cont.	80-way IDC Socket (Top Side)	51	GPIOB6 / T3PWM	GPIO / Timer 3 Output Trip
		52	GPIOB5 / PWM12	GPIO / PWM output pin 12
		53	GPIOB4 / PWM11	GPIO / PWM output pin 11
		54	GPIOB3 / PWM10	GPIO / PWM output pin 10
		55	GPIOB2 / PWM9	GPIO / PWM output pin 9
		56	GPIOB1 / PWM8	GPIO / PWM output pin 8
		57	GPIOB0 / PWM7	GPIO / PWM output pin 7
		58	DVCC_RTN	5V – use for off card Analog 5V
		59	RESET_INPUT*	Reset to DSP
		60	AGND	Analog Ground
		61	ADCINB5	Analog Input 5 for Sample and Hold B
		62	ADCINB4	Analog Input 4 for Sample and Hold B
		63	AGND	Analog Ground
		64	ADCINB3	Analog Input 3 for Sample and Hold B
		65	ADCINB2	Analog Input 2 for Sample and Hold B
		66	AGND	Analog Ground
		67	ADCINB1	Analog Input 1 for Sample and Hold B
		68	ADCINB0	Analog Input 0 for Sample and Hold B
		69	AGND	Analog Ground
		70	ADCINA0	Analog Input 0 for Sample and Hold A
		71	ADCINA1	Analog Input 1 for Sample and Hold A
		72	AGND	Analog Ground
		73	ADCINA2	Analog Input 2 for Sample and Hold A
		74	ADCINA3	Analog Input 3 for Sample and Hold A
		75	AGND	Analog Ground
		76	ADCINA4	Analog Input 4 for Sample and Hold A
		77	ADCINA5	Analog Input 5 for Sample and Hold A
		78	AGND	Analog Ground
		79	2.5V	2.5V Reference Output
		80	AGND	Analog Ground

Conn. No	Connector Type	Pin No.	Signal Name.	Comments
Hysteresis Controller / PWM Signals				
X4	MASCON5 (Molex 5-way Header)	1	HB1	Hysteresis Gate Signal 1
		2	HB2	Hysteresis Gate Signal 2
		3	HB3	Hysteresis Gate Signal 3
		4	HB4	Hysteresis Gate Signal 4
		5	GND	
Hysteresis Controller / PWM Signals				
X5	MASCON5 (Molex 5-way Header)	1	HB1A	Hysteresis Gate Signal 1A
		2	HB2A	Hysteresis Gate Signal 2A
		3	HB3A	Hysteresis Gate Signal 3A
		4	HB4A	Hysteresis Gate Signal 4A
		5	GND	

Appendix E CPLD Pin Definitions

Pin No.	Signal Name	Comments
1	SPISOMI	SPI data out – sourced from CPT-DA2810 Interface
2	SPISIMO	SPI data input – sourced from CPT-DA2810 Interface
3	PWMA8	PWMA output pin 8
4	PWMA7	PWMA output pin 7
5	PWMA6	PWMA output pin 6
6	PWMA5	PWMA output pin 5
7	PWMA4	PWMA output pin 4
8	PWMA3	PWMA output pin 3
9	3.3V	3.3V supply
10	GND	Digital Ground
11	GND	Digital Ground
12	PWMA2	PWM output pin 2
13	3.3V	3.3V supply
14	PWMA1	PWM output pin 1
15	CPLD_CS*	CPLD Chip Select
16	DIGIN8	Digital Input 8
17	DIGIN7	Digital Input 7
18	DIGIN6	Digital Input 6
19	DIGIN5	Digital Input 5
20	PWMB8	PWMB output pin 8
21	PWMB7	PWMB output pin 7
22	TMS	JTAG Enable
23	TDI	JTAG Input Signal
24	TCK	JTAG Clock Signal
25	TDO	JTAG Output Signal
26	MA2	Address Line 1 (MA_2)
27	MA1	Address Line 1 (MA_1)
28	MA0	Address Line 1 (MA_0)
29	WR*	MiniBus Write Signal
30	CS1*	Chip Select Line 1
31	3.3V	3.3V supply
32	GND	Digital Ground
33	CS0*	Chip Select Line 0
34	CS2*	Chip Select Line 2
35	MINI_MS*	Mini Bus Master/Slave mode selection
36	RD*	MiniBus Read Signal
37	GND	Digital Ground
38	D7	Address/Data Line 7
39	3.3V	3.3V supply
40	D6	Address/Data Line 6
41	D5	Address/Data Line 5
42	D4	Address/Data Line 4
43	D3	Address/Data Line 3
44	D2	Address/Data Line 2
45	3.3V	3.3V supply
46	GND	Digital Ground
47	D1	Address/Data Line 1
48	D0	Address/Data Line 0
49	MINIBUS*	Minibus Chip Select
50	RESET_MB*	Mini Bus Reset

Pin No.	Signal Name	Comments
51	XINT1B	Interrupt Input
52	MCLK	MCLK from DSP's CLKOUT
53	TEST_1	CPLD Test Point
54	GPIOF7	Spare IO Pin to/from CPT-DA2810
55	GPIOF1	Spare IO Pin to/from CPT-DA2810
56	EN_TTL*	SCIB TTL Mode Enable
57	H_ENAB*	Hysteresis Connectors enable
58	PDPINTB*	Gate Fault Trip Signal EVB
59	3.3V	3.3V supply
60	GND	Digital Ground
61	INDEXB	Interrupt Input
62	INDEXA	Interrupt Input
63	3.3V	3.3V supply
64	CLKOUT	Clock Signal from CPT-DA2810
65	GND	Digital Ground
66	PDPINTA*	Gate Fault Trip Signal EVA
67	XINT1A	Interrupt Input
68	N/C	No Connection
69	INB	Hysteresis Controller Analog Switch Source Selection
70	INA	Hysteresis Controller Analog Switch Source Selection
71	INC	Hysteresis Controller Analog Switch Source Selection
72	IND	Hysteresis Controller Analog Switch Source Selection
73	IN3	Hysteresis Controller Analog Switch Mode Selection
74	IN2	Hysteresis Controller Analog Switch Mode Selection
75	IN1	Hysteresis Controller Analog Switch Mode Selection
76	T3PWM/GPIOB6	Output from CPT-DA2810 (EVB)
77	T4PWM/GPIOB7	Output from CPT-DA2810 (EVB)
78	CAP4	EVB Capture 4 or Digital Input Connection
79	GND	Digital Ground
80	3.3V	3.3V supply
81	CAP5	EVB Capture 5 or Digital Input Connection
82	CAP6	EVB Capture 6 or Digital Input Connection
83	PWM1	PWM EVA input pin 1
84	PWM2	PWM EVA input pin 2
85	PWM3	PWM EVA input pin 3
86	PWM4	PWM EVA input pin 4
87	PWM5	PWM EVA input pin 5
88	3.3V	3.3V supply
89	PWM6	PWM EVA input pin 6
90	GND	Digital Ground
91	T1PWM	PWM EVA input pin 7
92	T2PWM	PWM EVA input pin 8
93	GND	Digital Ground
94	3.3V	3.3V supply
95	CAP1	EVB Capture 1 or Digital Input Connection
96	CAP2	EVB Capture 2 or Digital Input Connection
97	CAP3	EVB Capture 3 or Digital Input Connection
98	RESET*	CPLD Reset
99	XINT1	To External Interrupt 1 on CPT-DA2810 Interface
100	SPICLK	SPI Clock – sourced from CPT-DA2810 Interface

Appendix F Test Points on CPT-Mini2810

TEST POINT NAME	SIGNAL NAME	GRID REF.	DESCRIPTION
TP1	+5AVCC	**A2**	5V Analog Supply
TP2	AGND	**C2**	Analog Ground
TP3	TEST_1	**C6**	CPLD Test Point
TP4	3.3V	**D6**	3.3V locally generated supply
TP5	GND	**D7**	Digital Ground
TP6	DVCC	**D7**	5V regulated supply

Appendix G CPLD Registers

Function	*Register*	*SPI Address*	*Section*
Mini Bus– Address Range		0x00 – 0x8F	3.3.3
Serial Communications Interface B Mode Select	SCIBMODE	0xC2	3.3.4
Capture Port Mode Select	CAPQEP	0xC4	3.3.8.2
Interrupt XINT1 Select	INTSEL	0xC6	3.3.8.1
EVA Command Configuration	EVACOMCON	0xD0	3.3.9
EVA Deadband Generator	EVACONDB	0xD2	3.3.9
EVB Command Configuration	EVBCOMCON	0xD4	3.3.9.1
EVB Deadband Generator	EVBCONDB	0xD6	3.3.9.2
Analog Switch Selection	ANLGSW	0xD8	3.3.10[2]
General Purpose Digital I/O Pins	GPIO	0xDA	3.3.11

[2] This definition is available within the *CPT-Mini2810 Hysteresis Controller Technical Manual* available separately from Creative Power Technologies.

Appendix H CPLD Register Bit Definition - WRITE

BYTE 0								BYTE 1								BYTE 2							
MSB																							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCS1	SCS0	SMA4	SMA3	SMA2	SMA1	SMA0	R/W*	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X	X

BYTE	BIT(S)	NAME	DESCRIPTION
0	23 – 22	SCS1 – SCS0	Chip Select 00 Mini Bus address range CS0* 01 Mini Bus address range CS1* 10 Mini Bus address range CS2* 11 Additional CPLD Peripherals/Registers
	21 – 17	SMA4 – SMA0	Memory Address within the Chip Select Ranges
	16	R/W*	Read / Write* signal – decoded to separate CPLD outputs **0 Write mode (WR* = 0, RD* = 1)** 1 Read mode (WR* = 1, RD* = 0)
1	15 – 8	D7 – D0	Data Lines
2	7 – 0	X	Don't Care

Appendix I CPLD Register Bit Definition - READ

BYTE 0								BYTE 1								BYTE 2							
MSB																							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCS1	SCS0	SMA4	SMA3	SMA2	SMA1	SMA0	R/W*	X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

BYTE	BIT(S)	NAME	DESCRIPTION
0	23 – 22	SCS1 – SCS0	Chip Select 00 Mini Bus address range CS0* 01 Mini Bus address range CS1* 10 Mini Bus address range CS2* 11 Additional CPLD Peripherals/Registers
	21 – 17	SMA4 – SMA0	Memory Address within the Chip Select Ranges
	16	R/W*	Read / Write* signal – decoded to separate CPLD outputs 0 Write mode (WR* = 0, RD* = 1) **1 Read mode (WR* = 1, RD* = 0)**
1	15-8	X	Don't Card
2	7 – 0	D7 – D0	Data Lines – Read Data

Appendix J Mini Bus Registers – Address 0x00 – 0x8F

ADDRESS BYTE 0								DATA BYTE 1							
MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCS1	SCS0	SMA4	SMA3	SMA2	SMA1	SMA0	R/W*	D7	D6	D5	D4	D3	D2	D1	D0

BYTE	BIT(S)	NAME	DESCRIPTION
1	15 – 14	SCS1 – SCS0	Chip Select 00 CS0* (assert CPLD output pin LOW) 01 CS1* (assert CPLD output pin LOW) 10 CS2* (assert CPLD output pin LOW)
	13 – 12	SMA4 – SMA3	00
	11 – 9	SMA2 – SMA0	Memory Address within the Chip Select Range Maps directly to CPLD outputs MA2 – MA0
	8	R/W*	Read / Write* signal – decoded to separate CPLD outputs 0 Write mode (WR* = 0, RD* = 1) 1 Read mode (WR* = 1, RD* = 0)
	7 – 0	D7 – D0	Data Lines - decoded to/from CPLD data output pins D7 – D0

Appendix K SCIBMODE Register – Address 0xC2

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
SPD	X	X	X	X	X	X	SC
R/W-0	-0	-0	-0	-0	-0	-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	SPD	Internal Bidirectional SPI Switch enable (Special Function CPLD required) 0 Standard Operating Mode
	6 – 1	Reserved	
	0	SC	Serial Port B receive signal (SCIRXB) sourced from: 0 TTL – Plug-in TTL level Connector 1 485 – RS-485 Molex Connector

Appendix L CAPQEP Register – Address 0xC4

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	CP
-0	-0	-0	-0	-0	-0	-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7 – 1	Unused	
	0	CP	Capture Port Definition signal sourced from: 0 QEPB Mode: QEP allocated to EVB (ZX to EVA) 1 QEPA Mode: QEP allocated to EVA (ZX to EVB)

Appendix M INTSEL Register – Address 0xC6

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	I1B	X	X	X	I1A
-0	-0	-0	R/W-0	-0	-0	-0	R/W-1

Legend: R = Read Access, W = Write Access, -n value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7 – 5	Unused	
	4	I1B	Mini Bus interrupt source Mode (XINT1B) 0 Disabled 1 Enabled (only asserted if I1A = 0)
	3 – 1	Reserved	
	0	I1A	Interrupt header source Mode (XINT1A): 0 Disabled 1 Enabled (priority)

Appendix N EVACOMCON Register – Address 0xD0

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
T1M	P6	P5	P4	P3	P2	P1	ENA
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BIT(S)	NAME	DESCRIPTION
7	T1M	Output Mode Selection for PWMA7 and PWMA8 0 PWM7A/ PWM8A as Digital Outputs (pass through) 1 T1PWM as Complementary PWM on PWMA7 and PWMA8
6	P6	Output Mode Selection for PWMA6 0 Sourced from PWM6 Input (pass through) 1 Internal Computation
5	P5	Output Mode Selection for PWMA5 0 Sourced from PWM5 Input (pass through) 1 Internal Computation
4	P4	Output Mode Selection for PWMA4 0 Sourced from PWM4 Input (pass through) 1 Internal Computation
3	P3	Output Mode Selection for PWMA3 0 Sourced from PWM3 Input (pass through) 1 Internal Computation
2	P2	Output Mode Selection for PWMA2 0 Sourced from PWM2 Input (pass through) 1 Internal Computation
1	P1	Output Mode Selection for PWMA1 0 Sourced from PWM1 Input (pass through) 1 Internal Computation
0	ENA	PWM Output Enable 0 Disable – outputs P1-P6 and PWMA7 & PWMA8 are set to 0 1 Enable – outputs are set depending on status of P1-P6,T1M

Appendix O EVACONDB Register – Address 0xD2

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
EDBT	DBT3	DBT2	DBT1	DBT0	DBTPS2	DBTPS1	DBTPS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	EDBT	Enable Deadband Generator for T1M = 1, ignored if T1M = 0 0 Disabled 1 Enabled
	6 – 3	DBT3 – DBT0	Dead-band timer period. These bits define the period value of the 4-bit dead band timers
	2 – 0	DBTPS2 – DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 x = Device (CPU) clock frequency

Appendix P EVBCOMCON Register – Address 0xD4

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
T3M	X	X	X	X	X	X	ENB
R/W-0	-0	-0	-0	-0	-0	-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BIT(S)	NAME	DESCRIPTION
7	T3M	Output Mode Selection for PWMB7 and PWMB8 0 PWMB7/ PWMB8 as Digital Outputs (pass through) 1 T3PWM as Complementary PWM on PWMB7 & PWMB8
6-1	Reserved	
0	ENB	PWMB7/B8 Output Enable 0 Disable – PWMB7 & PWMB8 set to 0 if T3M = 1 1 Enable – PWMB7 & PWMB8 set on status of T3M

Appendix Q EVBCONDB Register – Address 0xD6

DATA BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
EDBT	DBT3	DBT2	DBT1	DBT0	DBTPS2	DBTPS1	DBTPS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	EDBT	Enable Deadband Generator for T3M = 1, ignored if T3M = 0 0 Disabled 1 Enabled
	6 – 3	DBT3 – DBT0	Dead-band timer period. These bits define the period value of the 4-bit dead band timers
	2 – 0	DBTPS2 – DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 x = Device (CPU) clock frequency

Appendix R ANLGSW Register – Address 0xD8

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
HE	IN3	IN2	IN1	IND	INC	INB	INA
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read Access, W = Write Access, -0 value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	HE	Hysteresis Enable 0 PWM Signals sourced from EVA inputs 1 PWM Signals sourced from Hysteresis input
	6	IN3	Hysteresis band error signal sourced from: 0 DAC4/MEAS4 1 (IN2=1) DAC1/MEAS1 (IN2=0) DAC3/MEAS3
	5	IN2	Hysteresis band error signal sourced from: 0 DAC3/MEAS3 1 DAC1/MEAS1
	4	IN1	Hysteresis band error signal sourced from: 0 DAC2/MEAS2 1 DAC1/MEAS1
	3	IND	Hysteresis input MEAS3 selected from analog: 0 ADC5 1 ADC8
	2	INC	Hysteresis input MEAS4 selected from analog: 0 ADC4 1 ADC12
	1	INB	Hysteresis input MEAS2 selected from analog: 0 ADC10 1 ADC11
	0	INA	Hysteresis input MEAS1 selected from analog: 0 ADC2 1 ADC3

Appendix S GPIO Register – Address 0xDA

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	T1D	F7D	D1D	X	T1	F7	D1
-0	R/W-0	R/W-1	R/W-1	-0	R/W-1	R/W-0	R/W-0

Legend: R = Read Access, W = Write Access, -n value after reset

BYTE	BIT(S)	NAME	DESCRIPTION
1	7	Reserved	
	6	T1D	Direction of CPLD Pin TP3 (pin 53) 0 = Input (Default), 1 = Output
	5	F7D	Direction of CPLD Pin GPIOF7 (pin 54) 0 = Input, 1 = Output (Default)
	4	D1D	Direction of CPLD Pin GPIOD1 (pin 55) 0 = Input, 1 = Output (Default)
	3	Reserved	
	2	T1	CPLD Pin TP3 (pin 53): Set to 0/1 if T1D=1, Value can be read if T1D=0
	1	F7	CPLD Pin GPIOF7 (pin 54): Set to '0' if F7D=1, Value can be read if F7D=0
	0	D1	CPLD Pin GPIOD1 (pin 55): Set to '0' if D1D=1, Value can be read if D1D=0

Appendix T DATELO Register – Address 0xFA

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
M	M	M	D	D	D	D	D
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

Legend: R = Read Access, W = Write Access, -n value after reset.
Note: Reset value determined by Programmed Date of the CPLD Code

Appendix U DATEHI Register – Address 0xFC

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Y	Y	Y	Y	Y	Y	Y	M
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

Legend: R = Read Access, W = Write Access, -n value after reset.
Note: Reset value determined by Programmed Date of the CPLD Code

BYTE	BIT(S)	NAME	DESCRIPTION
DATEHI	15 – 9	Y	Year – in binary format (0-127) (2000-2127)
	8	M	Month – in binary format (1-12)
DATELO	7 – 5	M	
	4 – 0	D	Day of the Month – in binary format (1 – 31)

Appendix V VERSION Register – Address 0xFE

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
V	V	V	V	V	V	V	V
R-0	R-0	R-1	R-0	R-0	R-0	R-0	R-1

Legend: R = Read Access, W = Write Access, -n value after reset.
Note: Reset value determined by Programmed Version of the CPLD Code

Appendix W SPECIAL Register – Address 0xF0

BYTE 1							
MSB							LSB
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read Access, W = Write Access, -n value after reset.
Note: Reset value determined by Programmed Version of the CPLD Code